PAC407 CMOS VGA DIGITAL IMAGE SENSOR

General Description:

The PAC407 is a highly integrated CMOS active-pixel image sensor that has a VGA resolution (644H x 484V or 640H x 480V). The PAC407 outputs 8-bit data with wide range of formats include RGB Raw Data, RGB565 and YCbCr422 through an 8-bit parallel data bus. It is available in 32-pin LCC and 22-pin CSP.

To have an excellent image quality, the PAC407 supports all require image processing functions, includes Automatic Exposure Control, Automatic White Balance, Gamma Correction, Color Saturation Correction, Edge Enhancement, Lens Shading Compensation and Defect Compensation. These functions are all programmable via I^2C^{TM} serial control bus.

Features:

- **VGA, QVGA, QQVGA (Sub-sampling) and Window Of Interest (WOI) outputs with 8-bit parallel data mode, the formats include:**
  - **Raw Data**
  - **RGB565**
  - **YCbCr422**
- **VGA resolution, ~1/4" Lens**
  - **644 x 484 pixels (Raw Data)**
  - **640 x 480 pixels (YUV/RGB)**
- **Bayer-RGB color filter array**
- **Continuous variable frame time(1/2sec~1/30sec)**
- **On-chip 10-bit pipelined A/D converter**
- **On-chip programmable gain amplifier**
  - **4-bit color gain amplifier (x1~x2)**
  - **4-bit global gain amplifier (x1~x2)**
- **Automatic image control functions:**
  - **AEC: Automatic Exposure Control**
  - **AWB: Automatic White Balance**
- **Image quality control:**
  - **Color Saturation**
  - **Gamma Correction**
  - **Sharpness (Edge Enhancement)**
  - **Smooth filter for skin**
- **Defect Compensation**
- **Lens Shading Compensation**
- **X Flip Function for mirrored image**
- **Digital Zoom (x2, x4)**
- **<25mA(~15 fps) power dissipation**
- **I^2C^{TM} Serial Interface**
- **Pin-to-pin compatible to OV7648**
  (Except for the polarity of RESET pin)

Key Specification:

Supply Voltage		2.8V to 3.3V
Resolution		640x480(YUV) or 644x484(Raw)
Array diagonal		4.5mm (~1/4"Optic)
Pixel Size		5.6μmx5.6μm
Frame rate		~30 fps
System clock		Up to 26 MHz
Max. pixel rate (YUV)		26 MHz
Sensitivity	**BCA**	1.4 V/Lux-Sec
	BCW	1.2 V/Lux-Sec
Color filter		RGB Bayer Pattern
Exposure Time		~ 4us to 0.1412s
Scan Mode		Progressive
S/N Ratio		> 45 dB
Package	**BCA**	32-pin LCC
	BCW	22-pin CSP

Note1: Only 2 decouple-capacitors needed.
Note2: Excellent sensitivity.

1. Pin Assignment

1.1. PAC407BCW pin assignment

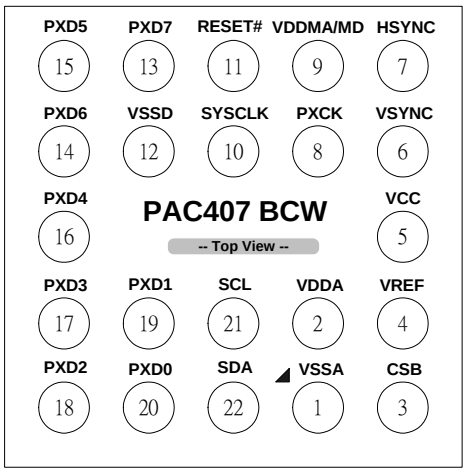


Figure 1.1. PAC407BCW pin assignment

Pin No.	Name	Type	Description
1	VSSA	GND	Analog ground.
2	VDDA	PWR	Connected with a 0.1uF capacitor
3	PWDN	IN	Power Down (chip power down when high).
4	VREF	IN	Internal voltage reference.
5	VCC	PWR	N.C.
6	VSYNC	OUT	Vertical synchronization signal.
7	HSYNC	OUT	Horizontal synchronization signal.
8	PXCK	OUT	Pixel clock output.
9	VDDMA/MD	PWR	Main Power (include IO pad power), 2.8V to 3.3V.
10	SYSCLK	IN	Master clock input.
11	RESET#	IN	Resets all registers to their default values (chip reset when low).
12	VSSD	GND	Digital ground.
13	PXD7	OUT	Digital data out.
14	PXD6	OUT	Digital data out.
15	PXD5	OUT	Digital data out.
16	PXD4	OUT	Digital data out.
17	PXD3	OUT	Digital data out.
18	PXD2	OUT	Digital data out.
19	PXD1	OUT	Digital data out.
20	PXD0	OUT	Digital data out.
21	SCL	IN	I^2C^{TM} clock.
22	SDA	I/O	I^2C^{TM} data. Internal pull high resister is 10KΩ.

1.2. PAC407BCA

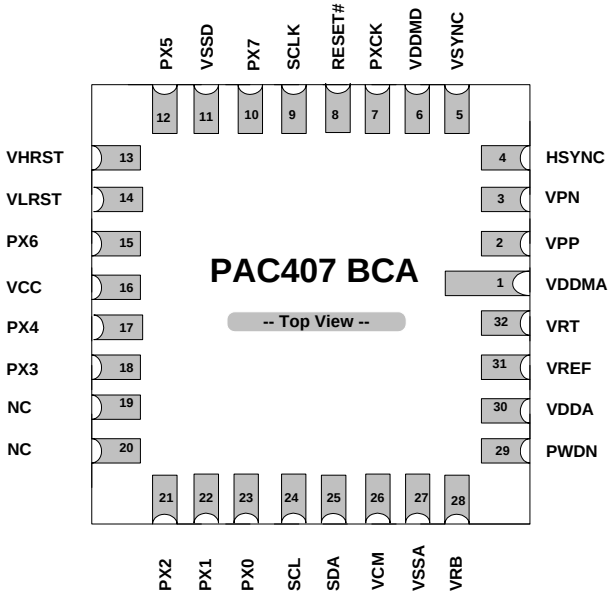


Figure 1.2. PAC407BCA pin assignment

Pin No.	Name	Type	Description
1	VDDMA	PWR	Main analog power, 2.8V to 3.3V.
2	VPP	BYPASS	Analog test output P
3	VPN	BYPASS	Analog test output N
4	HSYNC	OUT	Horizontal synchronization signal.
5	VSYNC	OUT	Vertical synchronization signal.
6	VDDMD	PWR	Main digital power (include IO pad power), 2.8V to 3.3V.
7	PXCK	OUT	Pixel clock output.
8	RESET#	IN	Resets all registers to their default values (chip reset when low).
9	SCLK	IN	Master clock input.
10	PX7	OUT	Digital data out.
11	VSSD	GND	Digital ground.
12	PX5	OUT	Digital data out.
13	VHRST	BYPASS	Test pin
14	VLRST	BYPASS	Test pin
15	PX6	OUT	Digital data out.
16	VCC	PWR	N.C.
17	PX4	OUT	Digital data out.
18	PX3	OUT	Digital data out.
19	NC	-	-
20	NC	-	-
21	PX2	OUT	Digital data out.
22	PX1	OUT	Digital data out.
23	PX0	OUT	Digital data out.
24	SCL	IN	I^2C^{TM} clock.

25	SDA	I/O	I^2C^{TM} data. Internal pull high resister is 10KΩ.
26	VCM	BYPASS	Voltage common mode
27	VSSA	GND	Analog ground.
28	VRB	BYPASS	Voltage reference bottom
29	PWDN	IN	Power Down (chip power down if high).
30	VDDA	PWR	Connected with a 0.1uF capacitor
31	VREF	IN	Internal voltage reference.
32	VRT	BYPASS	Voltage reference top

Note: The pin-out difference between PAC407BCA and PAS302BCA are pin1 and pin32.

2. Block Diagram

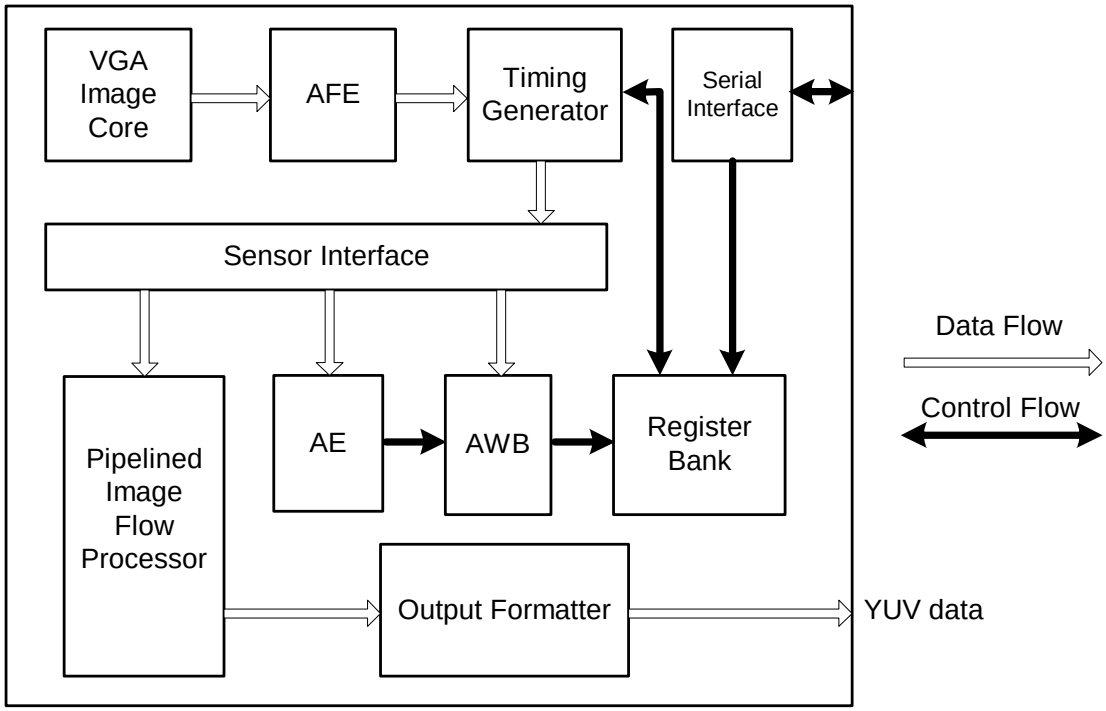


Figure 2.1. PAC407 block diagram

The PAC407 is a 1/4" CMOS imaging sensor with 644x488 physical pixels. The active region of sensor array is 644x484. The sensor array is cover with Bayer pattern color filters and micro-lens. The first pixel location <0,0> is programmable in 2 direction (X and Y) and the default value is at the left-down side of sensor array.

After a programmable exposure time, the signals of image are sampled first with CDS (Correlated Double Sampling) block to improve S/N ratio and reduce fixed pattern noise (FPN).

Three analog gain stages are implemented before signals are transferred to 10-Bit ADC. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B, G and R color. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

After three gain stages, the signals will be digitized by the on-chip 10-Bit ADC. After the image data have been digitized, further adjustment to the signal can be applied before the data is output to next stage.

3. Function Description

■ Defect Compensation

The Defect Compensation block can detect the possible defect pixel and replace it with average output of like-colored pixels from near side of defect pixel. This function can be programmed to enable/disable by user.

■ Hardware Windowing

Users are allowed to define window size and window location in PAC407. The location of window can be anywhere in the sensor array. Window location and size are determined by different register settings.

■ Sub-Sampling

PAC407 can be programmed to output image in QVGA, QQVGA and CIF size. In QVGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/2, while in QQVGA sub-sampling mode, both vertical and horizontal pixels are sub-sampling at 1/4.

■ Digital Zoom

By programming Hardware Windowing registers and Sub-sampling registers, PAC407supports 2X and 4X digital zoom.

■ Automatic White Balance

In digital image applications, color balance is typically achieved by automatic white balance (AWB). PAC407 can adjust its color spectrum sensitivity to the scene such that the resulting image on the average has an equal amount of all color components. The AWB mechanism can be set and adjusted by registers.

■ Color Saturation

If one color is more saturated than others, it will dominate the image. If the colors aren't saturated enough, the image might appear lifeless. Hence, PAC407 can enable color saturation function by setting registers to provide a more vivid image for user.

■ Lens Shading Compensation

In order to compensate the effect of the attenuation due to poorly optic component, PAC407 has a series of registers to eliminate the shading effect.

■ Gamma Correction

To realize a more brilliant image quality, PAC407 includes gamma correction function. Gamma correction performs on the luminance element of the image and allows compensating for non-linear dependence of the display device output against driving signal (ex. monitor brightness against CRT voltage). Gamma correction curve is shown as below, and some dedicated registers can adjust it.

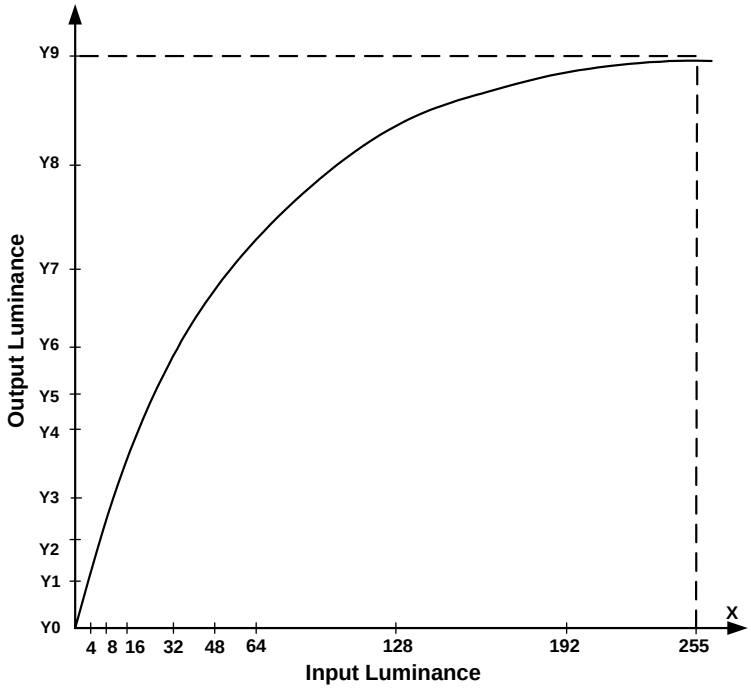


Figure 4.1 Gamma Correction curve

■ Power Down Mode

Because PAC407 is divided by two portions: Sensor and ASIC (ISP), software power down procedure should be performed on both portions. The PAC407 supports 2 power-down modes:

- Software power down

  Setting register "ISP_EnH"=0 in ASIC and register "Sw_PwrDn"=1 in Sensor.

- Hardware power down

  Pull PWDN pin to high to power down the chip. The chip will go into standby state.

■ Reset Mode

The PAC407 can be reseted by setting registers or by pulling low RESET# pin. PAC407 supports 2 reset modes:

- Software reset

  Setting register "Sw_Reset"=1 in Sensor and register "Software_Reset"=1 in ASIC to reset all the I^2C^{TM} registers.

- Hardware reset

  Pulling RESET# pin to low to reset the entire chip.

4. Output Format

4.1. Sensor Output Format

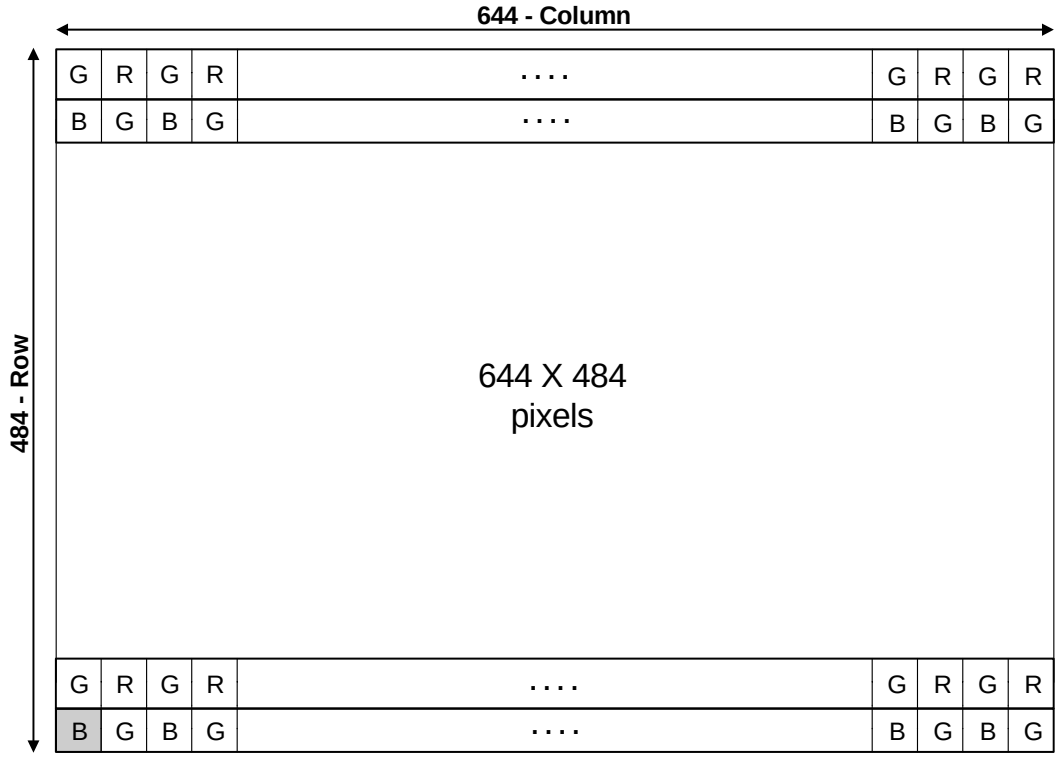


Figure 4.1 RAW data output

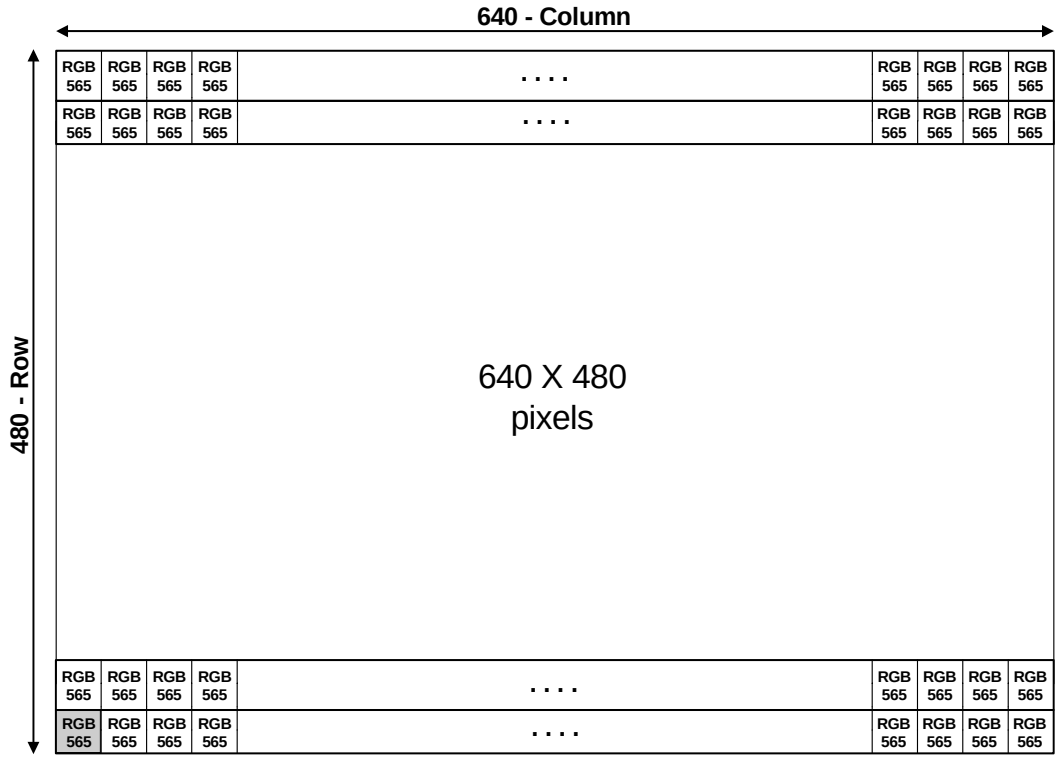


Figure 4.2 RGB565 output

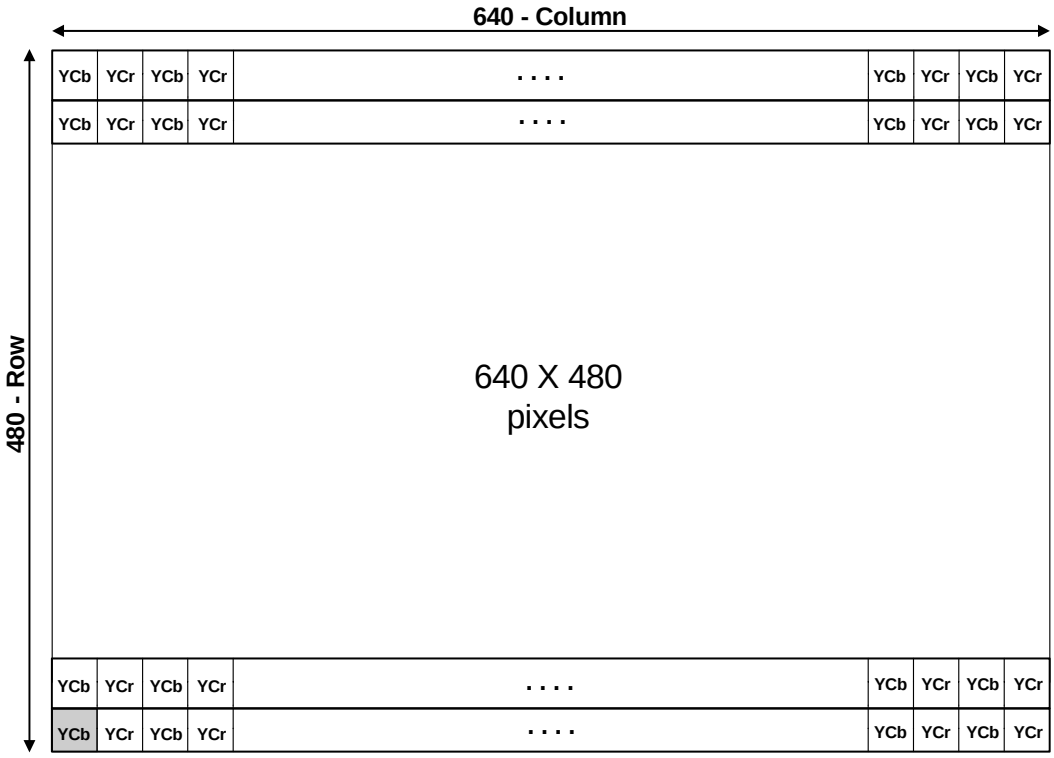


Figure 4.3 YCbCr422 Output

4.2. Output Timing

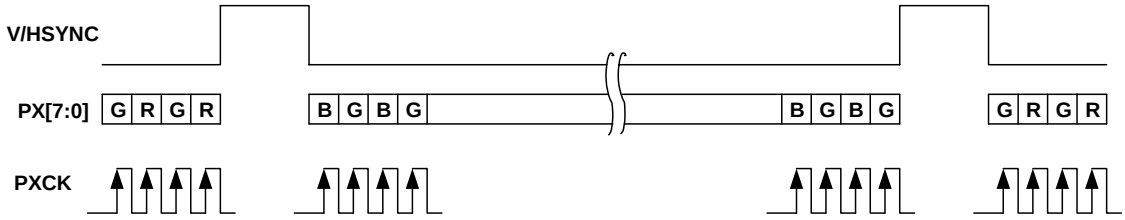


Figure 4.4 Inter-Line Timing

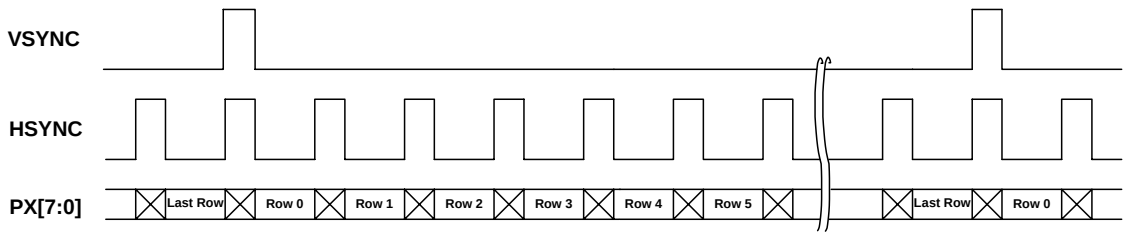


Figure 4.5 Inter-Frame Timing

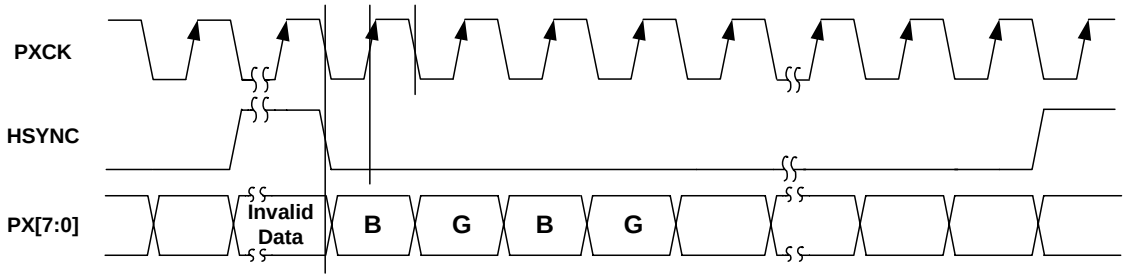


Figure 4.6 RAW Data Output Timing

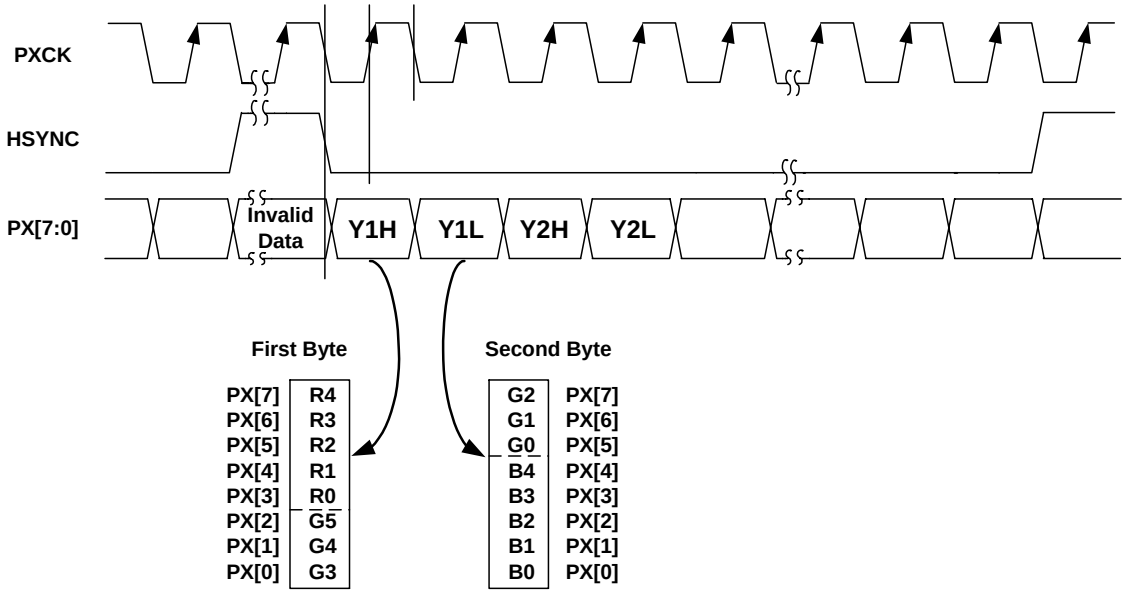


Figure 4.7 RGB565 Output Timing

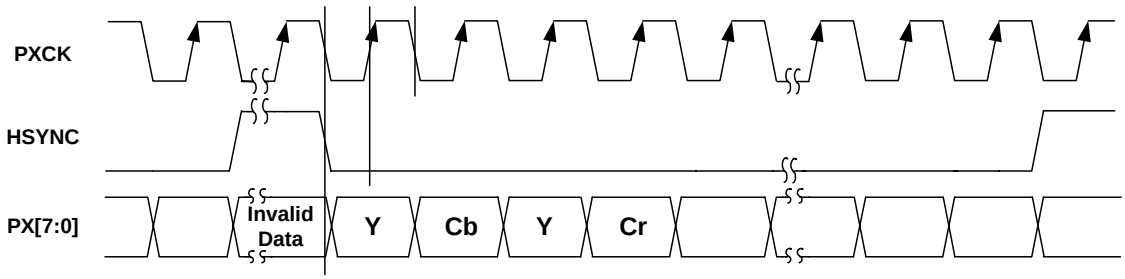


Figure 4.8 YCbCr422 Output Timing

Since the output stream of YCbCr422 or RGB565 format is two times then sensor raw data output, we should double the pixel clock rate while data format is in YCbCr422 or RGB565 mode.
The minimum of Np=1 in sensor timing generator that means the pixel clock rate is the same as system clock rate. Noticed that Np=1 can only be used in sensor raw data mode. When PAC407 is operated in YCbCr422 or RGB565 mode, the minimum of Np should be 2. Besides, when Np is odd number, the duty cycle of PXCK will not be 50%.
Note: The detail timing description for raw data output format could be found in PAS302 spec.

5. I^2C^{TM} Bus

PAC407 supports I^2C^{TM} bus transfer protocol and acts as slave device. The 7 bits unique slave address is 1000000 and the bus supports receiving / transmitting speed up to 400kHz.

5.1. I^2C^{TM} Bus Overview

There are only two lines SDA (serial data) and SCL (serial clock) carry information between the devices which are connected by I^2C^{TM} bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
Only the master can initiate a transfer (start), generate clock signals, and terminate a transfer (stop).
Start Condition :
A high to low transition of the SDA line while SCL is high defines a start condition.

Stop Condition :
A low to high transition of the SDA line while SCL is high defines a stop condition.

Valid Data:
The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte.
Both the master and slave can transmit and receive data from the bus.

Acknowledge :
The receiving device should pull down the SDA line during high period of the SCL clock line when a byte was transferred completely by transmitter. When in the case of that a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

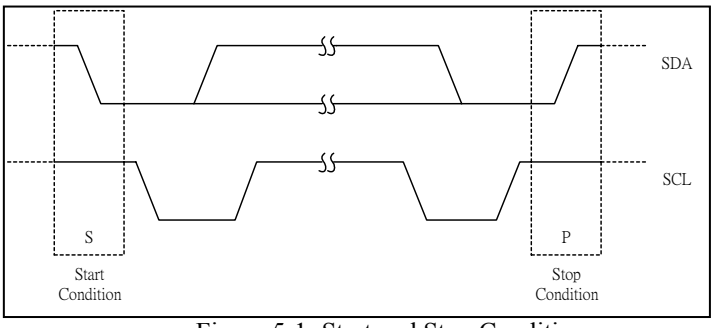


Figure 5-1: Start and Stop Conditions

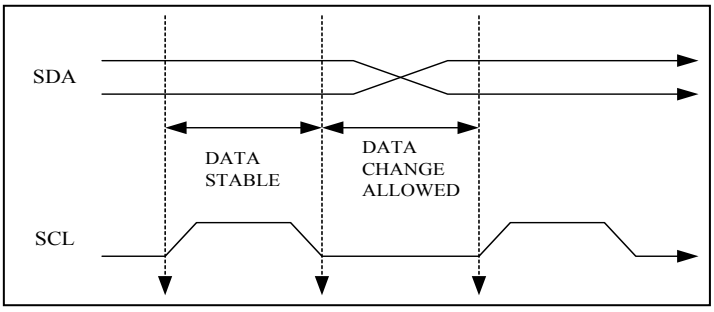
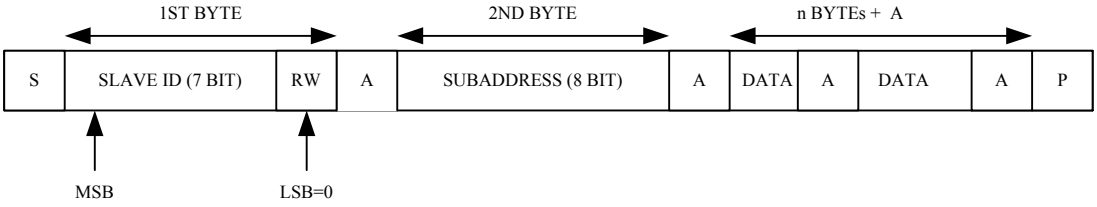


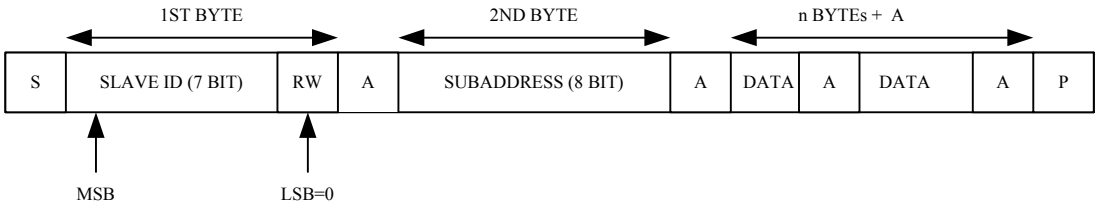
Figure 5-2: Valid Data

5.2. Data Transfer Format

5.2.1. Master transmits data to slave (write cycle)

- S: Start
- A: Acknowledge by slave
- P: Stop
- RW: The LSB of 1ST byte to decide whether current cycle is read or write cycle.
  If RW=1 that means read cycle, if RW=0 that means write cycle.
- SUBADDRESS: The address values of PAC407 internal control registers (Please refer to PAC407 register description)

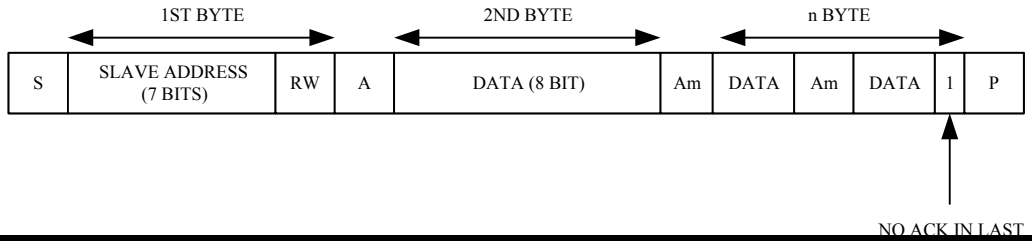




During the write cycle, the master generates start condition and then places the 1st byte data that combined slave address (7 bits) with a read/write control bit on SDA line. After slave(PAC407) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. And then following the slave's(PAC407) acknowledgment, the master places the 8 bits data on SDA line and transmit to PAC407 control register (address was assigned by 2nd byte). After PAC407 issue acknowledgment, the master can generate a stop condition to end this write cycle. In the condition of multi-byte write, the PAC407 sub-address will be increased automatically after each DATA byte has been transferred. The Data and A cycles are repeated until last byte write. Every control registers value inside PAC407 can be programming via this way. (Please refer to Figure 5.3.)

5.2.2. Slave transmits data to master (read cycle)

- The sub-address was assigned by previous write cycle
- The sub-address is automatically increased after each byte read
- Am : Acknowledged by master
- Note there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that combine slave address (7 bits) with a read/write control bit to SDA line. After slave issue acknowledgment, 8 bits DATA was placed on SDA line by PAC407. The 8 bit data was read from PAC407 internal control register that address was assigned by previous write cycle. Following the master acknowledgment, the PAC407 place the next 8 bits data (address is increased automatically) on SDA line and then transfer to master serially. The DATA and Am cycles are repeated until the last byte read. After last byte read, Am is no longer generated by master but instead of keeping SDA line as high. The slave (PAC407) must releases SDA line back to master to generate STOP condition. (Please refer to Figure 5.3.)

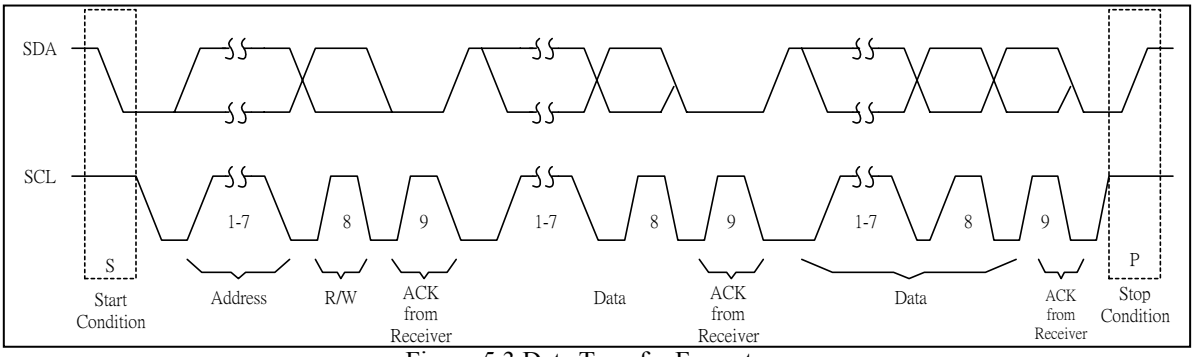


Figure 5.3 Data Transfer Format

5.3. I^2C^{TM} Bus Timing

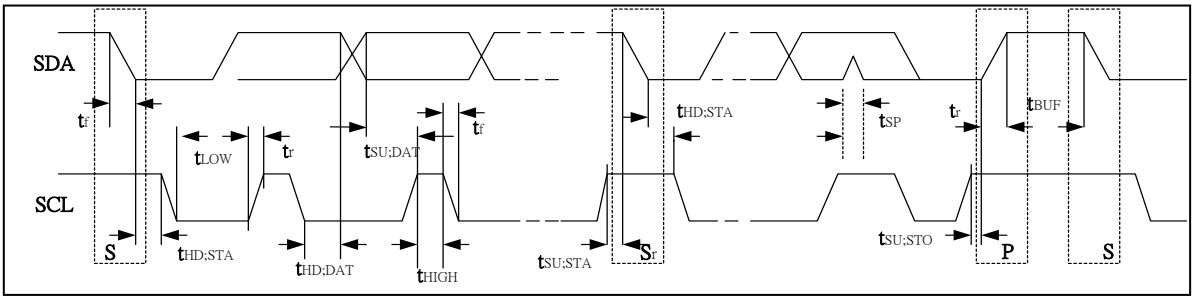


Figure 5.4 I^2C^{TM} Bus Timing

5.4. I^2C^{TM} Bus Timing Specification

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{scl}	10	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock	t_{LOW}	4.7	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I^2C^{TM} bus device	$t_{HD;DAT}$	0	3.45	µs
Data set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	30	N.D. (note)	ns
Fall time of both SDA and SCL signals	t_f	30	N.D. (note)	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START	t_{BUF}	4.7	-	µs

Capacitive load for each bus line	C_b	1	15	pF
Noise margin at LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	-	V
Noise margin at HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	-	V

Note: It depends on the "high" period time of SCL.

6. Electrical Characteristics

■ Absolute Maximum Ratings

Ambient Storage Temperature		-40℃ ~ +125℃
Supply Voltages (with respect to Ground)	**V_{CC}**	3V
	V_{DDA}	3V
	V_{DDMA}	4V
	V_{DDMD}	4V
All Input / Output Voltages (with respect to Ground)		-0.3V to V_{DDMD} + 1V
Lead Temperature, Surface-mount process		+230℃
ESD Rating, Human Body model		2000V

■ DC Electrical Characteristics (Ta =0℃ ~ 70℃)

Symbol	Parameter			Min.	Typ.	Max.	Unit
Type: PWR							
V_{DDA}	DC Supply voltage – Analog Power			2.4	2.5	2.6	V
V_{CC}	DC Supply voltage – Digital Power			2.4	2.5	2.6	V
$V_{DDMA/MD}$	DC Supply voltage – Main Analog/Digital			2.8	-	3.3	V
I_{DD}	Operating Current	$V_{DDMA/MD}$ = 3.3V	15 fps	-	24.4	-	mA
I_{PWDN}	Power Down Current	$V_{DDMA/MD}$ = 3.3V	15 fps	-	35	-	μA
Type: IN & I/O Reset and SYSCLK							
V_{IH}	Input voltage HIGH			0.7 x V_{DDMD}			V
V_{IL}	Input voltage LOW					0.3 x V_{DDMD}	V
C_{IN}	Input capacitor					10	pF
Type: OUT & I/O for PXD0:7, PXCK, H/VSYNC & SDA, load 10pf, 1.2kΩ,2.5volts							
V_{OH}	Output voltage HIGH			0.9 x V_{DDMD}			V
V_{OL}	Output voltage LOW					0.1 x V_{DDMD}	V

■ AC Operating Condition

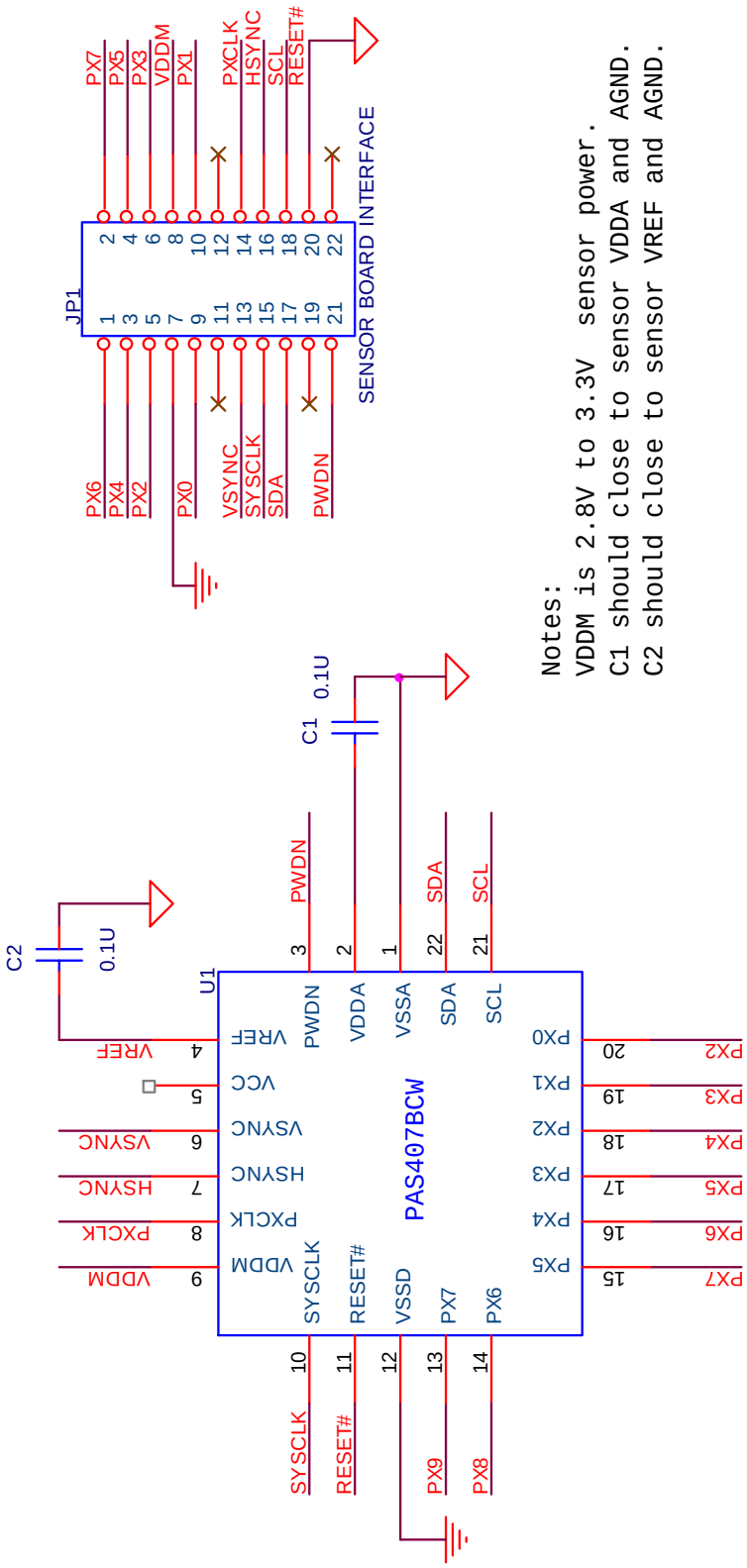
Symbol	Parameter	Min.	Typ.	Max.	Unit
SYSCLK	Master clock frequency			26	MHz
PXCK	Pixel clock output frequency (when YUV out)			26	MHz

■ Sensor Characteristics

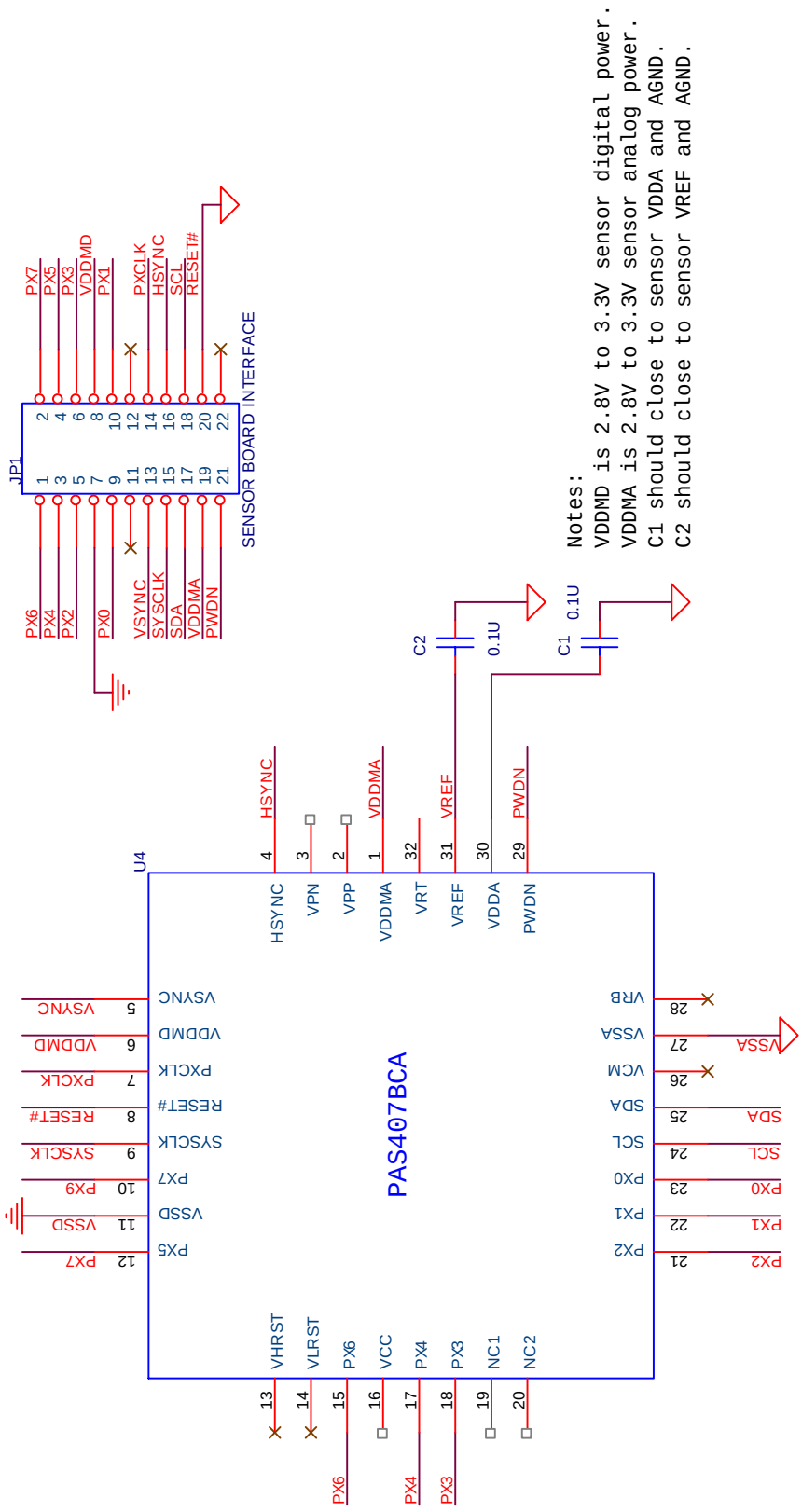
Parameter		Typ.		Unit	Note
		BCA	BCW		
Sensitivity		1.4	1.2	V/Lux-Sec	
Signal to Noise Ratio		> 45		dB	
Dynamic Range		60		dB	
Temperature Range	Operation	-10 ~ 70		℃	
	Stable Image	0 ~ 50			

7. Reference Circuit Schematic

7.1. PAC407BCW



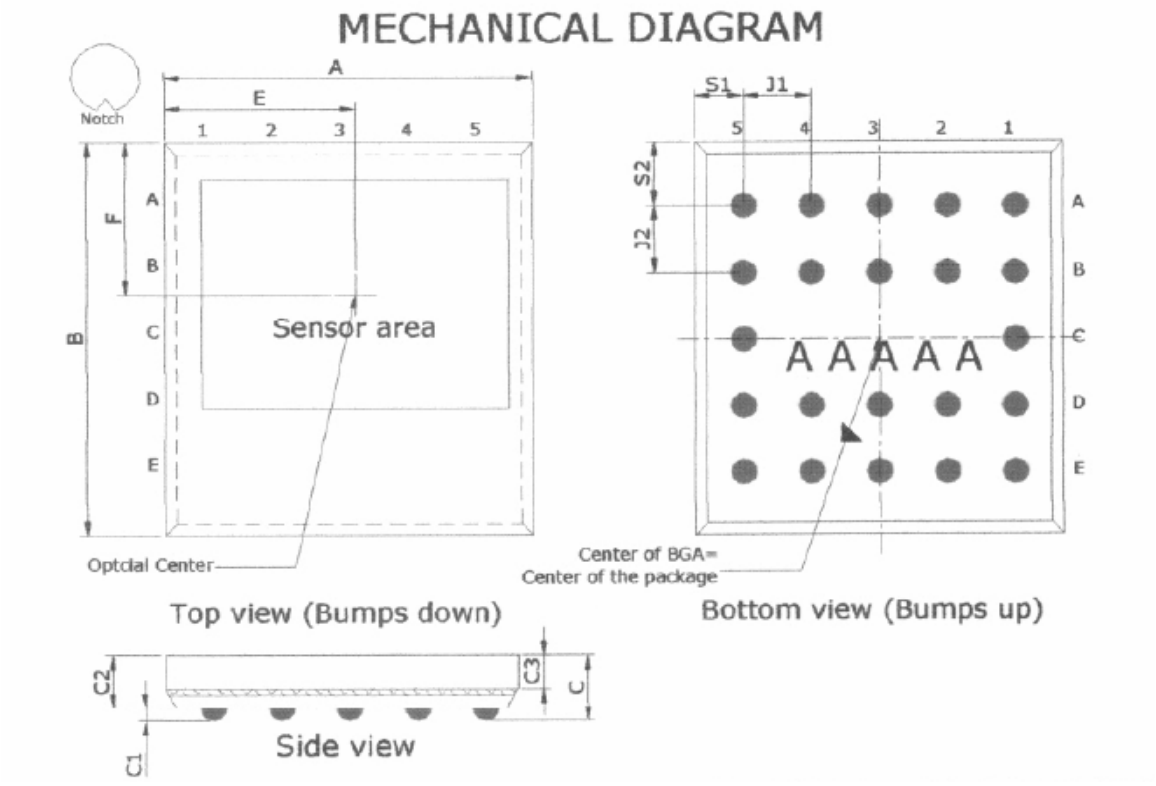
7.2. PAC407BCA



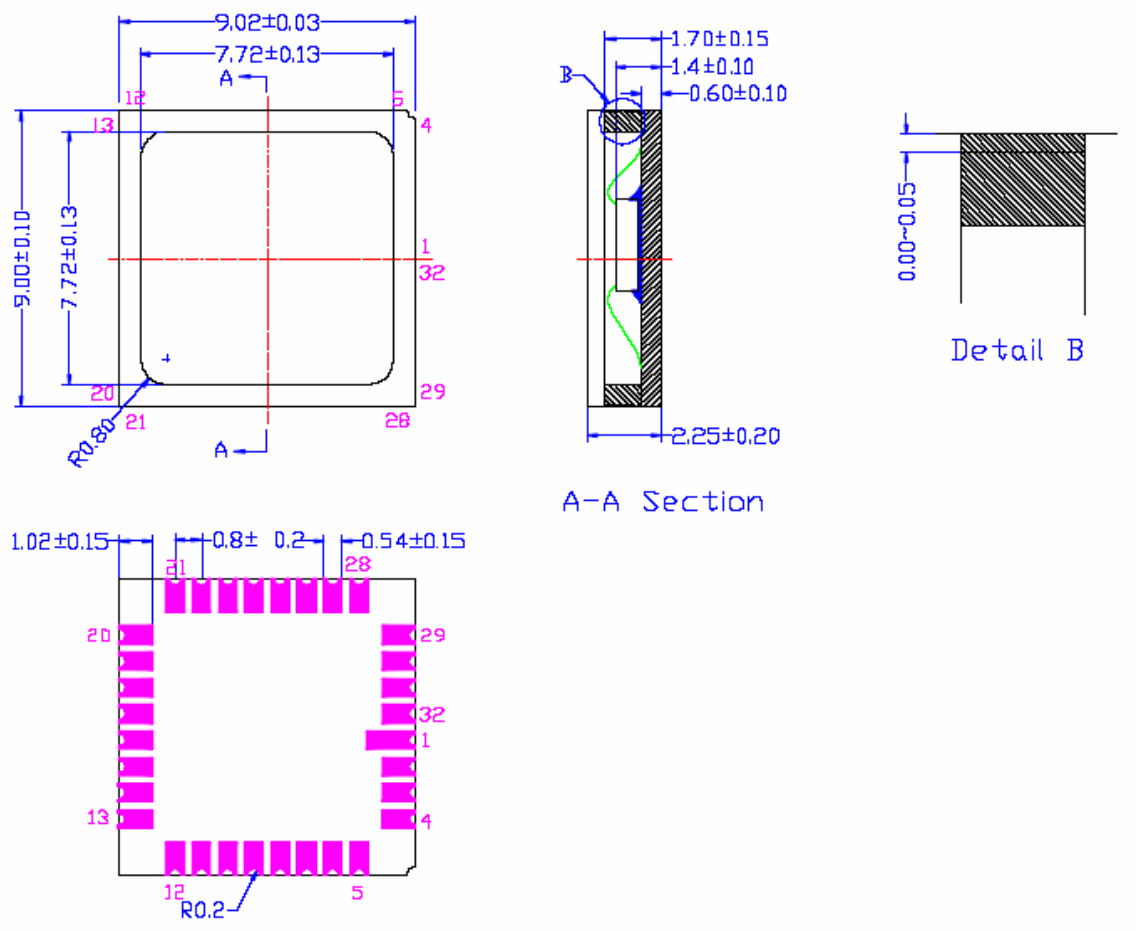
8. **Package** Specification

8.1. PAC407BCW

Dimensions	Symbol	Nominal	Min.	Max.	Unit
Package Body Dimension X	A	4340	4315	4365	µm
Package Body Dimension Y	B	4755	4730	4780	µm
Package Height	C	800	740	860	µm
Ball Height	C1	160	130	190	µm
Package Body Thickness	C2	640	605	675	µm
Thickness of Glass surface to wafer	C3	415	395	435	µm
Ball Diameter	D	300	270	330	µm
Total Pin Count	N	22	-	-	Ball
Pin Count X axis	N1	5	-	-	µm
Pin Count Y axis	N1	5	-	-	µm
Pin Pitch X axis	J1	800	-	-	µm
Pin Pitch Y axis	J2	800	-	-	µm
Edge to Pin Center Distance along X	S1	570	540	600	µm
Edge to Pin Center Distance along Y	S2	777.5	747.5	807.5	µm
Edge to Optical Center Distance along X	E	2254.16	2229.16	2279.16	µm
Edge to Optical Center Distance along Y	F	1832.84	1807.84	1857.84	µm



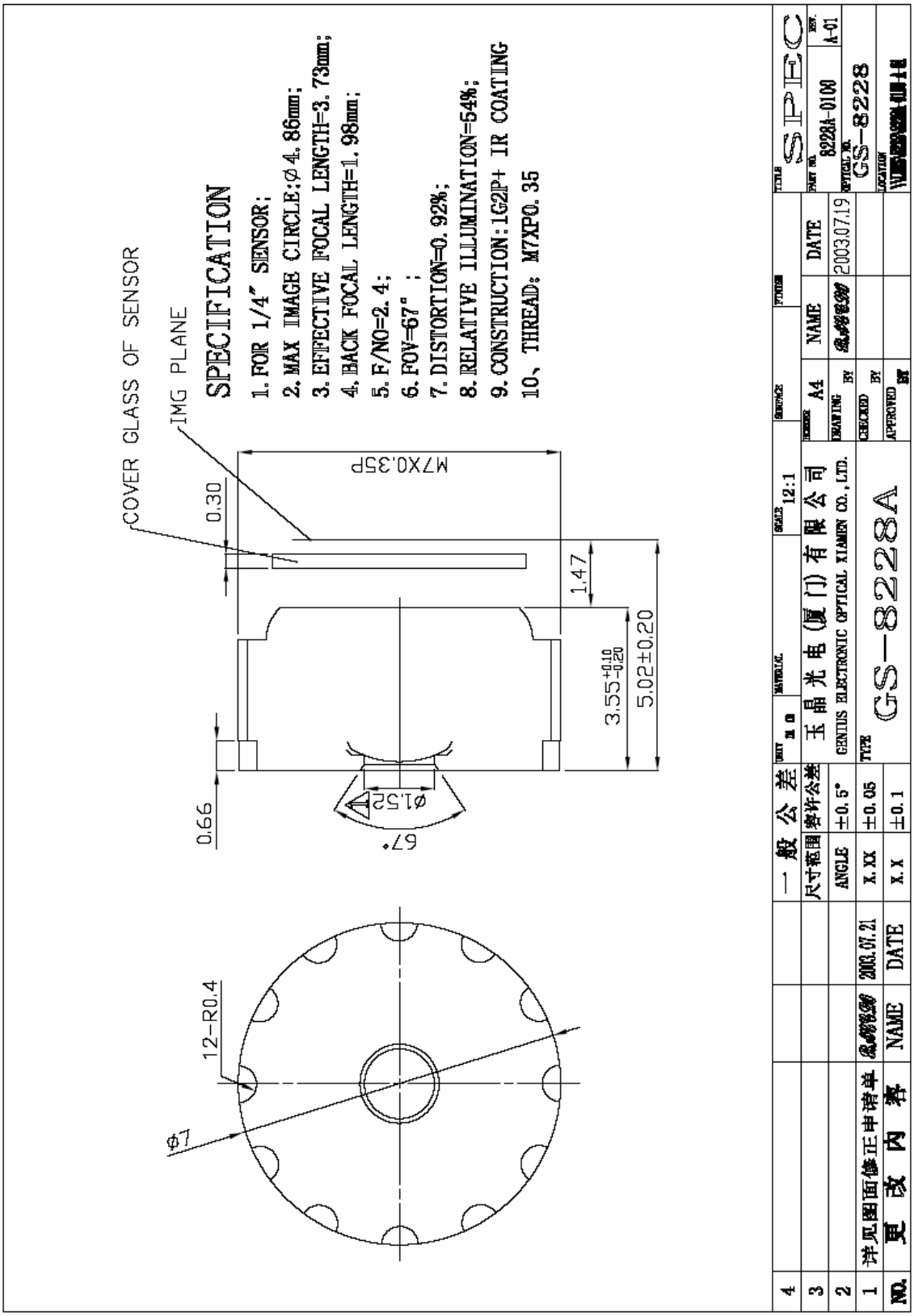
8.2. PAC407BCA

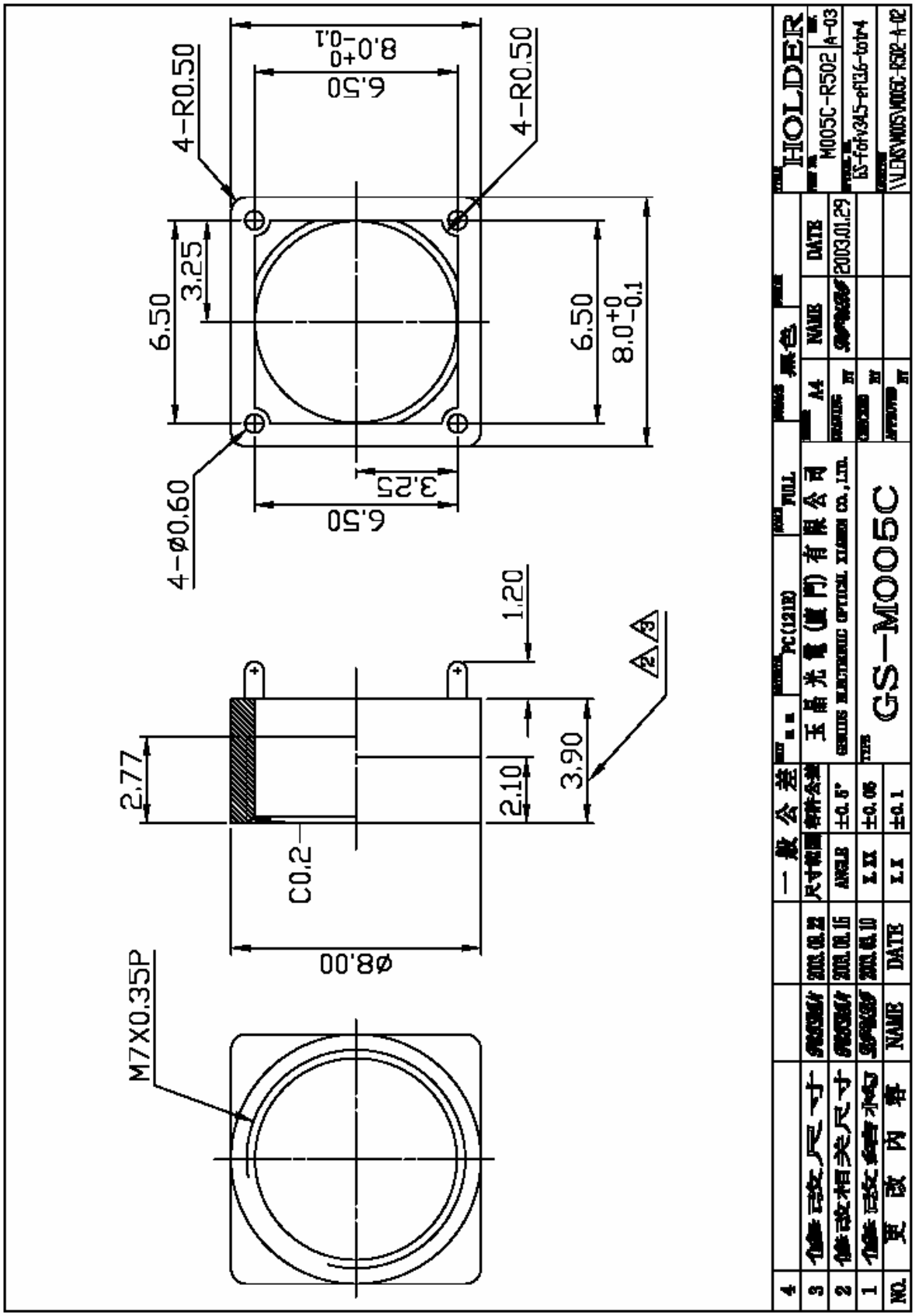


Unit:mm

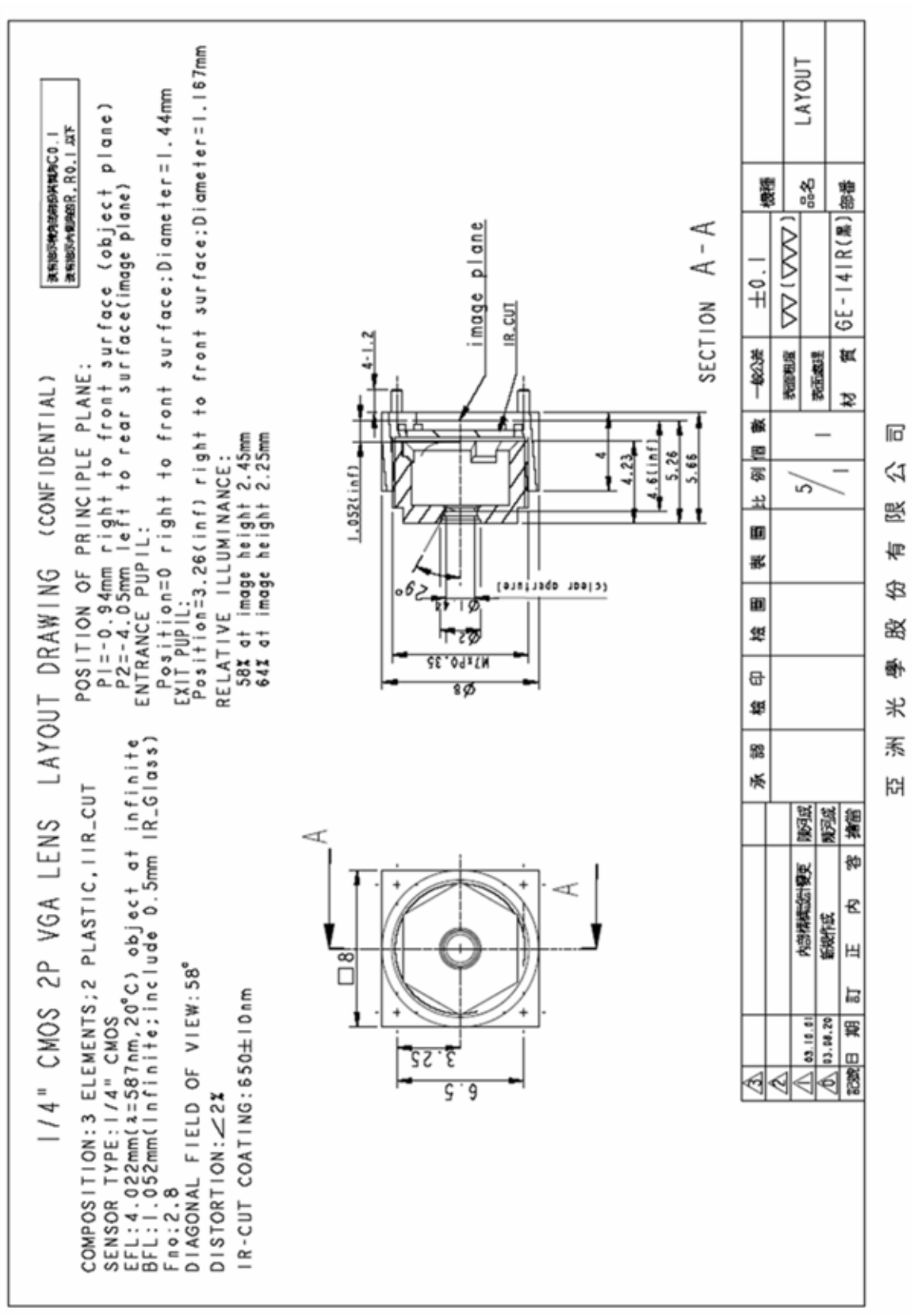
9. Recommended Lens and Holder

9.1. Genius Lens（2P1G）




4-R0.50
4-R0.50
8.0+0 -0.1
6.50
3.25
6.50
6.50
8.0+0 -0.1
3.25
6.50
4-ø0.60
1.20
2.77
2.10
3.90
C0.2
ø8.00
M7X0.35P
HOLDER
GS-M005C
玉晶光電(蘇州)有限公司
M005C-R502
2003.01.29

9.2. Asia-optical Lens（2P）



9.3. MaxEmil Lens（3P）

