Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

The PT2249A_PT2250A Series are infra-red remote control receivers utilizing CMOS Technology. Remote Control System can be constructed together with the PT2248 remote control encoder. The PT2249A Series are packaged in 16 pins DIP (PT2249A version is also available in SOP package) and are capable of controlling 10 functions while the PT2250A Series are packaged in 24 pins DIP and are capable of controlling 18 functions. Several options, inverting/non-inverting IR signal input and/or dependent/independent cyclic (toggle) outputs, are provided to fit different application needs.

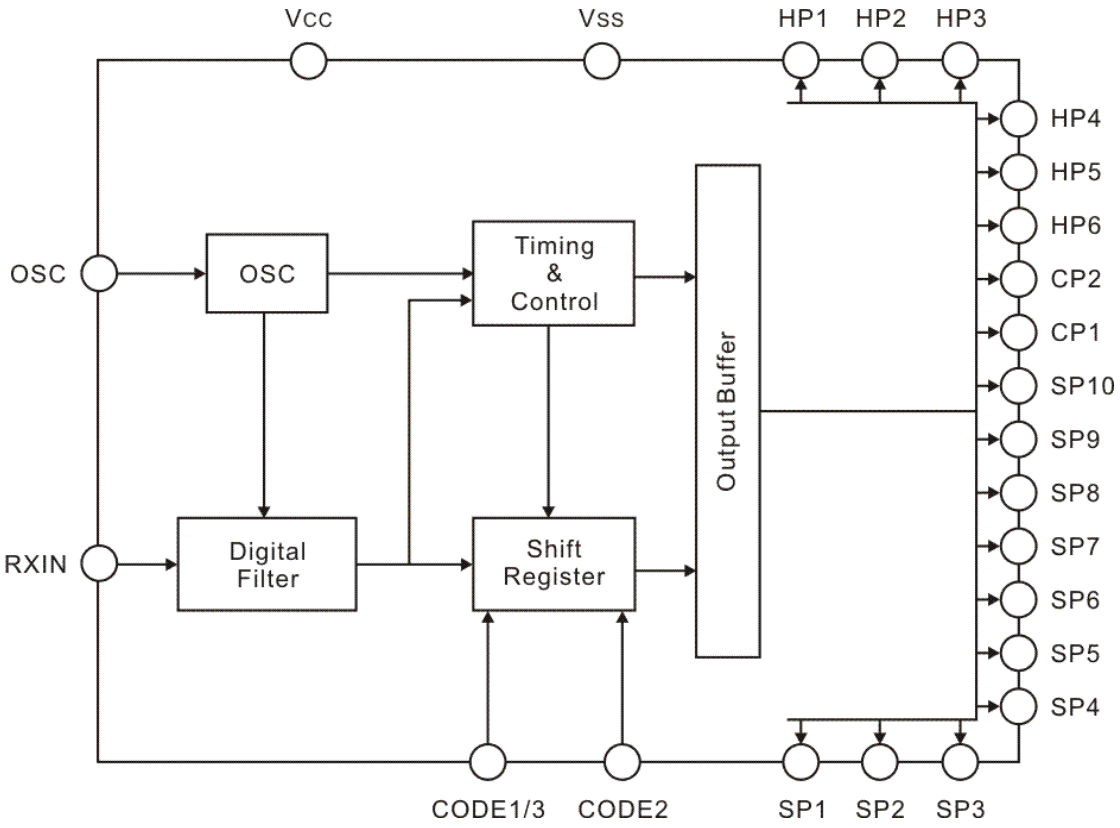
FEATURES

- CMOS technology
- Low power consumption
- Very high noise immunity
- Able to output parallel multiple keying signals sent from the transmitter (PT2249A is able to output up to 5 functions simultaneously while PT2250A is able to output up to 6 functions simultaneously)
- Outputs for single pulse, hold pulse and cyclic pulse are provided
- A single terminal type oscillator by means of RC is provided
- Code detection circuit prevents interference from various types of machines and apparatus
- Digital filtering and code checking prevent interference from light sources such as PL lamp without sacrificing the receiving sensitivity

APPLICATIONS

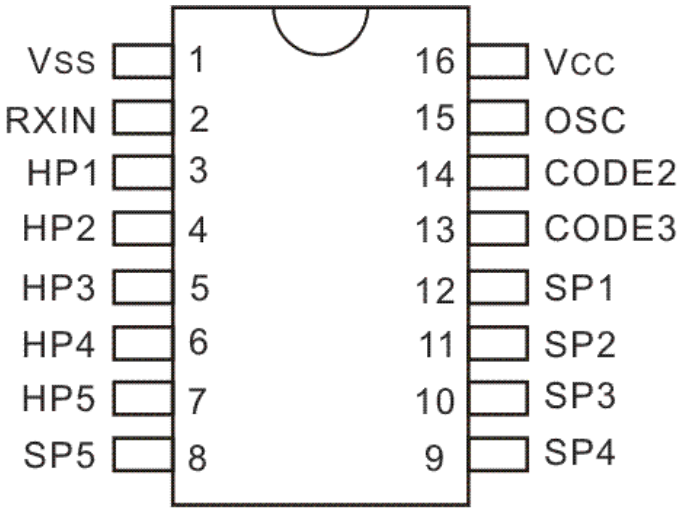
- Audio equipment remote control
- Television (TV) remote control
- Video Cassette Recorder (VCR) remote control

BLOCK DIAGRAM

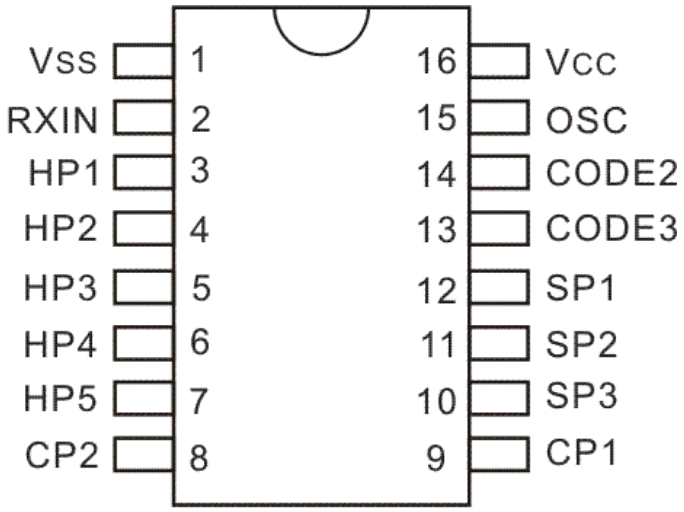


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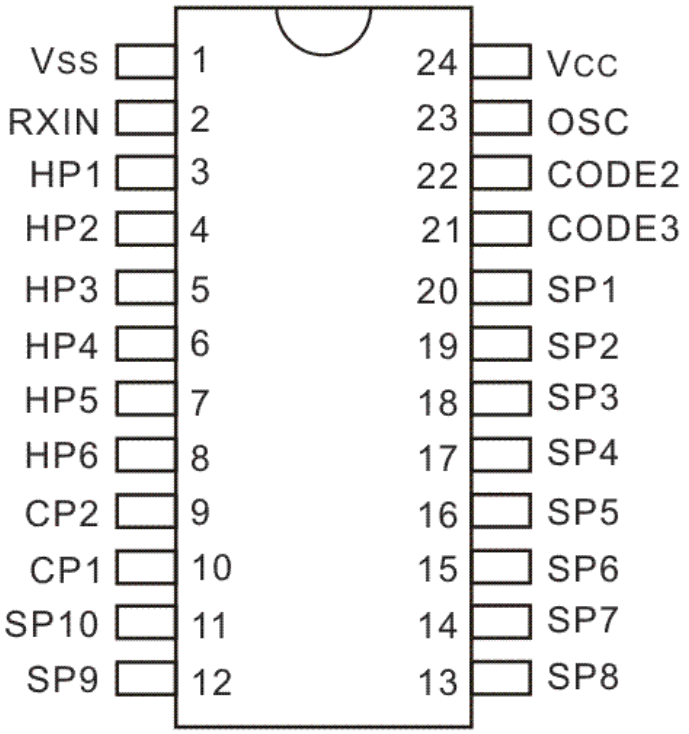
PIN CONFIGURATIONS



PT2249A
PT2249A-SN



PT2249AL
PT2249AHN



PT2250A

PIN DESCRIPTION

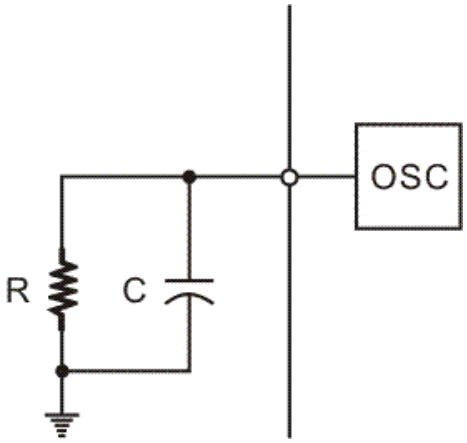
Pin Name	Pin No.			I/O	Description
	PT2249A PT2249A-SN	PT2249AL PT2249AHN	PT2250A		
Vss	1	1	1	-	Negative Power Supply
RXIN	2	2	2	I	Receiver Input. Instruction signal with carrier wave eliminated should be inputted to this pin. Input signal may be optionally inverted before fed into internal decoding circuit.
HP1 ~ HP5	3 ~ 7	3 ~ 7	3 ~ 7	O	Hold Pulse. As long as proper signal is received, this output is held at "H" level. (approximately 160ms will be "0" after key is released.)
HP6	-	-	8	O	
CP1	-	9	10	O	Cyclic Pulse. When receiving signal is inputted, CP1/CP2 is inversed. CP1 output may be optionally governed by (dependent to) the output state of CP2. See Functional Description for details.
CP2	-	8	9	O	
SP1 ~ SP3	12 ~ 10	12 ~ 10	20 ~ 18	O	Single Pulse. When the receiving signal is inputted, the active output will be at "H" level only for a fixed duration of time (approximately 107 msec), then it will return to "L" level.
SP4	9	-	17	O	
SP5	8	-	16	O	
SP6 ~ SP10	-	-	15 ~ 11	O	
CODE1	-	-	22	I	Tx/Rx Matching Code. Transmitter Code is compared with a code set at this terminals and if matched, input is accepted.
CODE2	14	14	21	I	
CODE3	13	13	-	I	
OSC	15	15	23	I/O	OSC Input/Output. A resistor and a capacitor are in parallel connection between this terminal and Vss.
Vcc	16	16	24	-	Positive Power Supply

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FUNCTIONAL DESCRIPTION

OSCILLATION CIRCUIT

Timing with transmitter signal and internal operating clock are all decided by this oscillator.
Using CMOS Technology, the oscillator of PT2248 transmitter is constructed through a combination of a linear amplifier by connecting C and R between the oscillator terminal and Vss.



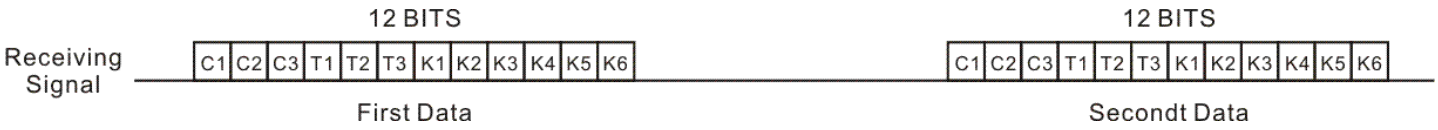
Notes:
1. R=39K±5%
2. C=100pF±5%

RECEIVING SIGNAL INPUT CIRCUIT

The signal is received by IR receiver module and the wave is infused into the IC.
The RXIN has a built-in Schmitt trigger circuit for shaping received signal waveform to eliminate rounding. PTC has made available various options to suit IR receiving module with positive or negative output. PT2249A Series / PT2250A Series with “N” Option was specially designed for IR modules with negative output. PT2249A Series / PT2250A Series without the “N” Option were specially designed for IR receiving modules with positive output. In these two options, IR signals without external inversion can be fed into the RXIN directly.

RECEIVING SIGNAL CHECK

The receiving signal check is used to check 2 cycle transmitting signals sent from the transmitter to determine if it is a normal signal.



First, the data is stored in the 12-bit shift register. Then, when the second data is pushed into the shift register, the data is forced out of the shift register by one bit where the first data has been stored. The "pushed out" data and the incoming data are checked to see if they match. If there is an error in the receiving signal of the 12-bit data check, the system is reset at that point. Conversely, when all receiving data are checked OK, (HP1 ~ HP6 signals) outputs are raised from "L" level to "H" level.

CODE COMPARISON

To prevent interference with other models: C1, C2, and C3 code bits are provided to check whether the transmitter and receiver codes match.

It is only when both codes match that the internal latch strobe pulse is generated to latch the receiving data. The output is then raised from "L" level to "H" level. If both codes do not match, no latch strobe pulse is generated and the output remains at "L" level (HPs and SPs) or unchanged (CPs).

The Code Bits used differ depending on the receiver. Please refer below.

Rx / PT2248 Code Pin	PT2249A	PT2250A
T1 (C1 Code)	Diode	C1
T2 (C2 Code)	C2	C2
T3 (C3 Code)	C3	Diode

Note: where C1, C2, C3 will be "1" if one diode is connected between CODE and Tn pins; n=1 to 3 in PT2248; otherwise will be set to "0".

CODING

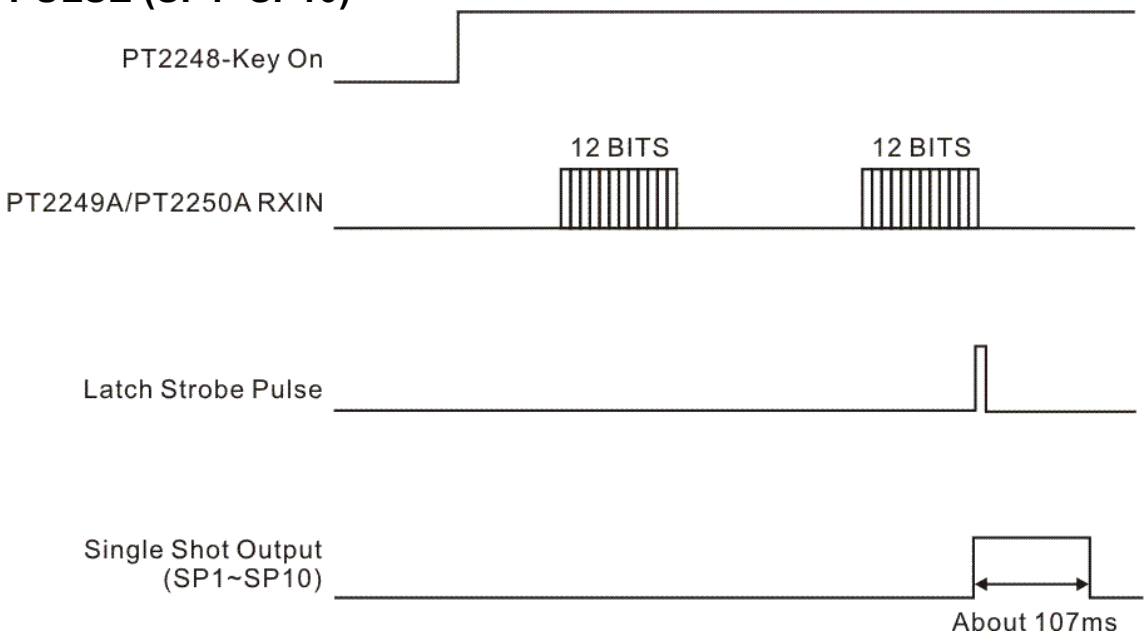
CODE1, CODE2 and CODE3 are internally pulled up to Vcc by pull-up resistors.

To encode each code bit to “1”:
Open the corresponding CODE pin, or Insert a capacitor between CODE pin and Vss.

To encode each Code bit to “0”:
Connect the corresponding CODE pin to Vss.

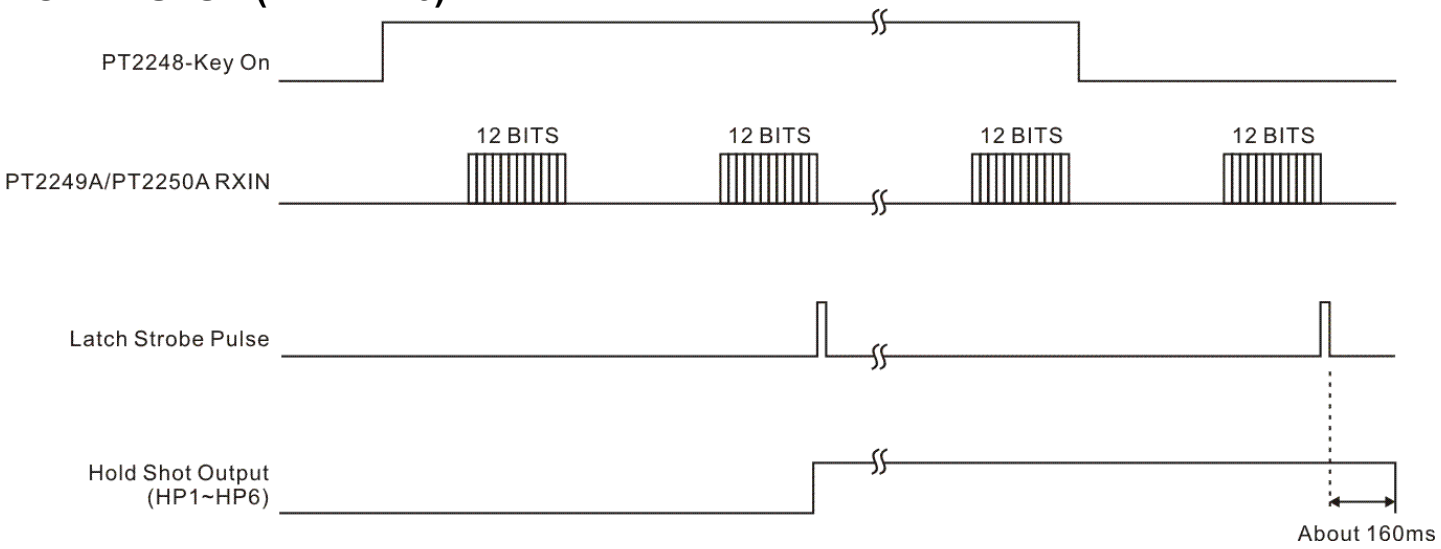
EXPLANATION OF OUTPUT TYPES: SP, HP AND CP

SINGLE PULSE (SP1~SP10)

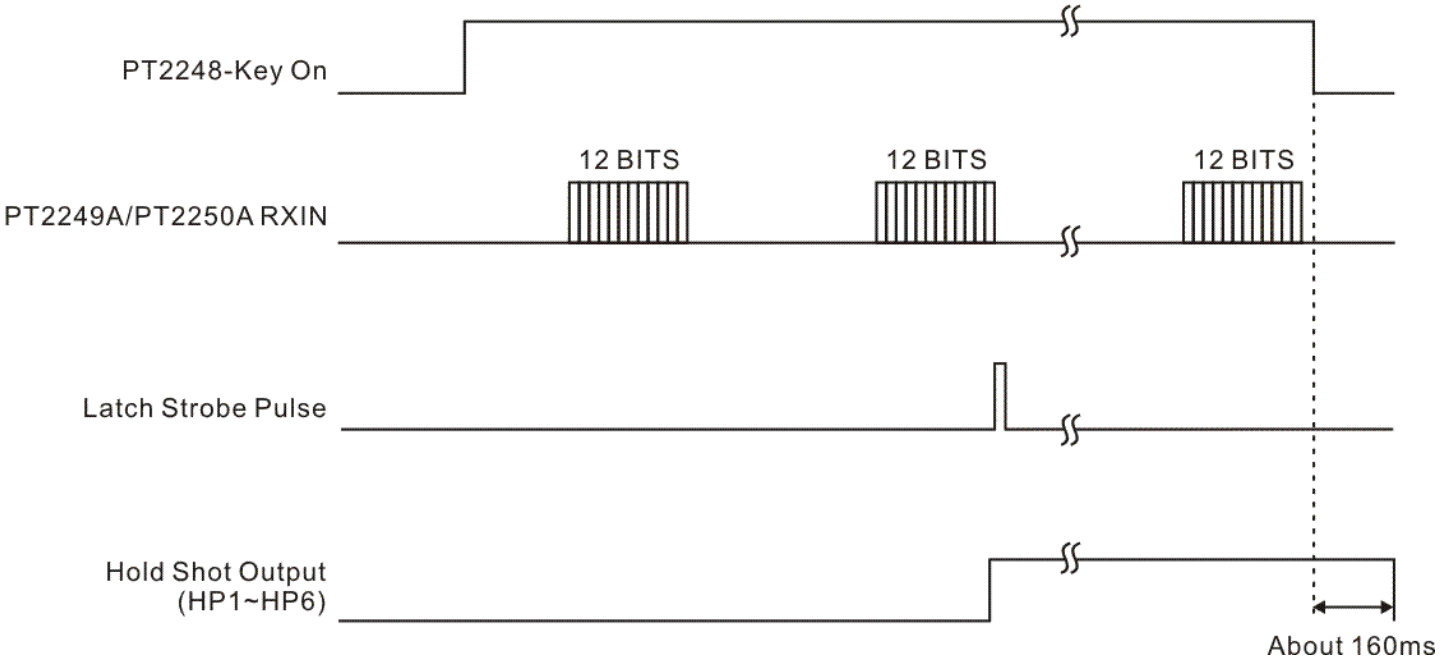


If there is no error in the receiving signal of the 12-bit data check, it will generate a single pulse output.

HOLD PULSE (HP1~HP6)



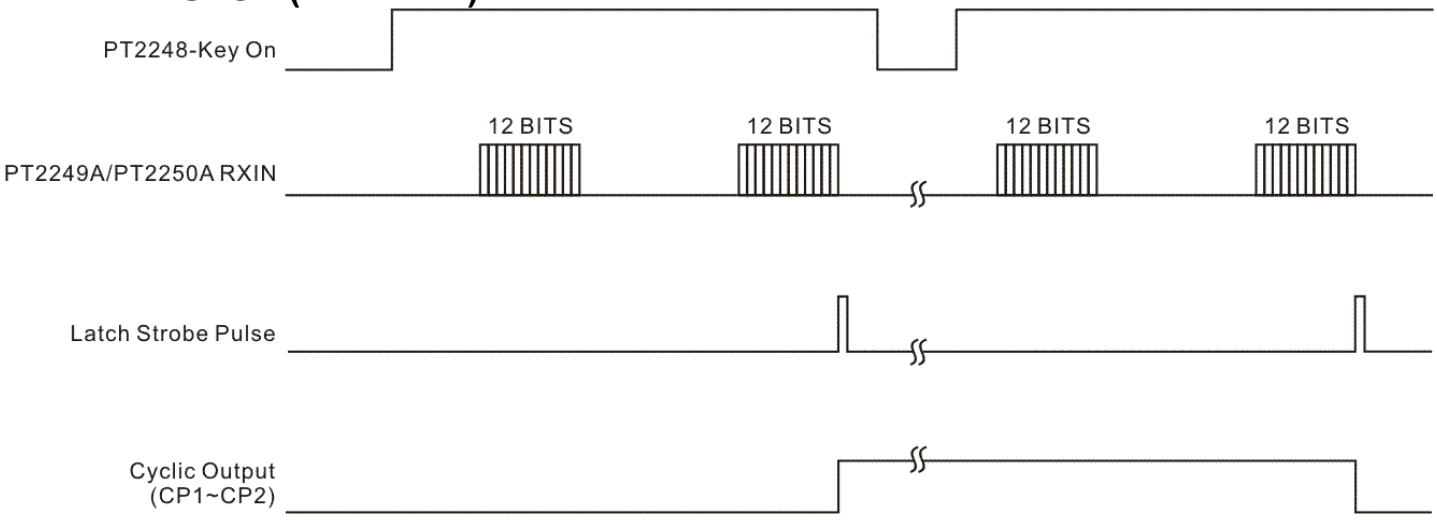
Normally, after two matched code words (12-bit per word) transmitted from PT2248 is detected, the latch strobe is generated, thereby producing a latch strobe pulse. This causes an “H” state output and this output is sustained at “H” level as long as the continuous signal received. Approximately 160ms after the key is released and the continuous signal is stopped, the output is reversed to “L” level by above the last latch strobe pulse. Please refer to the diagram



Under abnormal conditions where intolerable interference of any kind would cause the receiver to receive only one matched code word during the last transmission (please refer to the diagram above), then approximately 160ms after the key is released and the hold shot output (continuous signal) is stopped, the output is reversed to “L” level.

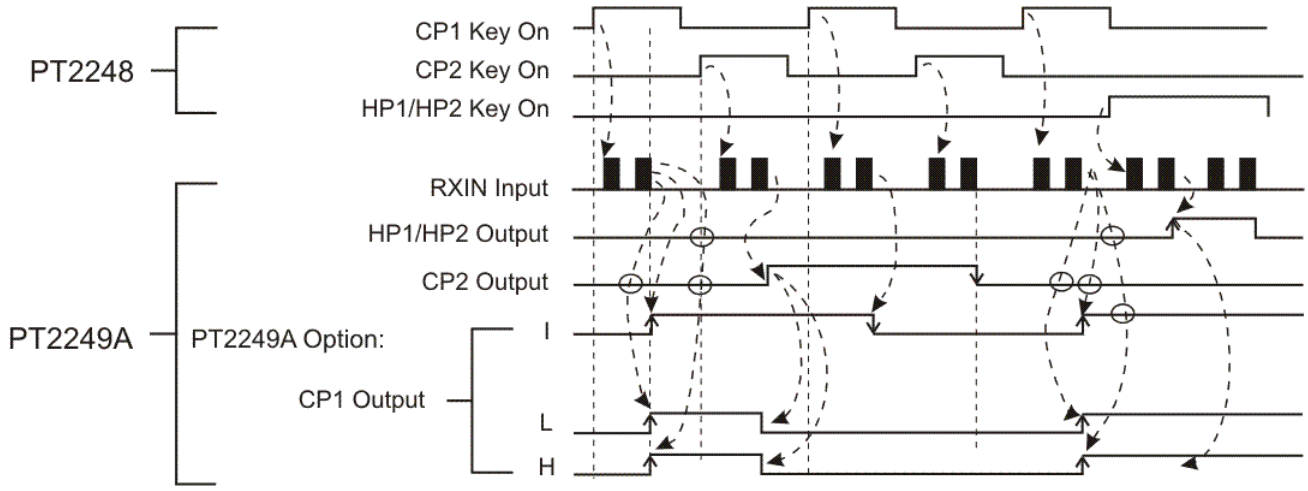
Under any condition, the HP1 ~ HP6 are able to drive simultaneously a maximum of six outputs at “H” Level by the continuous signals sent from the transmitter. These functions are most applicable for REC-PLAY, REC-PAUSE and CUE/REVIEW of the Tape Deck.

CYCLIC PULSE (CP1~CP2)



When signal is received, the cyclic pulse output is reversed. This cyclic pulse is used for Power ON/OFF, MUTE, etc.

The relationship between CP1 and CP2 (in the PT2249A Series) is shown in the diagram below:



PT2249AL:

- CP1 may not be set to “H” level when CP2 is in “H” Level.
- CP1 is reset to “L” level whenever CP2 is set to “H” level.

PT2249AHN:

- CP1 may not be set to "H" Level when CP2 or HP1 or HP2 is in "H" Level.
- CP1 is reset to "L" Level whenever CP2 or HP1 or HP2 is set to "H" Level.

*CODE ALLOCATION**

*** NOTE: KEY NO. IS OF PT2248**

Key No.	PT2248 Data Bit									Function of Instruction (PT2249A or PT2250A O/P)	
	H	S1	S2	D1	D2	D3	D4	D5	D6		
	T1	T2	T3	K1	K2	K3	K4	K5	K6		
1	1	0	0	1	0	0	0	0	0	Continuous Signal	HP1
2	1	0	0	0	1	0	0	0	0	Continuous Signal	HP2
3	1	0	0	0	0	1	0	0	0	Continuous Signal	HP3
4	1	0	0	0	0	0	1	0	0	Continuous Signal	HP4
5	1	0	0	0	0	0	0	1	0	Continuous Signal	HP5
6	1	0	0	0	0	0	0	0	1	Continuous Signal	HP6
7	0	1	0	1	0	0	0	0	0	Single-Shot Signal	SP1
8	0	1	0	0	1	0	0	0	0	Single-Shot Signal	SP2
9	0	1	0	0	0	1	0	0	0	Single-Shot Signal	SP3
10	0	1	0	0	0	0	1	0	0	Single-Shot Signal	SP4
11	0	1	0	0	0	0	0	1	0	Single-Shot Signal	SP5
12	0	1	0	0	0	0	0	0	1	Single-Shot Signal	SP6
13	0	0	1	1	0	0	0	0	0	Single-Shot Signal	SP7
14	0	0	1	0	1	0	0	0	0	Single-Shot Signal	SP8
15	0	0	1	0	0	1	0	0	0	Single-Shot Signal	SP9
16	0	0	1	0	0	0	1	0	0	Single-Shot Signal	SP10
17	0	0	1	0	0	0	0	1	0	Cyclic Signal	CP1
18	0	0	1	0	0	0	0	0	1	Cyclic Signal	CP2

C1 ~ C3 Code Bits are available in addition to the above data bits for optional Code Selection.

PT2250A can use all keys.
PT2249A are able to use Key No. 1 ~ 5 and Key No. 7 ~ 11.
PT2249A/AL/AHN can use Key No. 1 ~ 5, Key No. 7 ~ 9, and Key No. 17 ~ 18.

ABSOLUTE MAXIMUM RATING

(Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.5	V
Input/Output voltage	V_{IN}	Vss-0.5 to Vcc+0.5	V
Power dissipation	Pd	200	mW
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

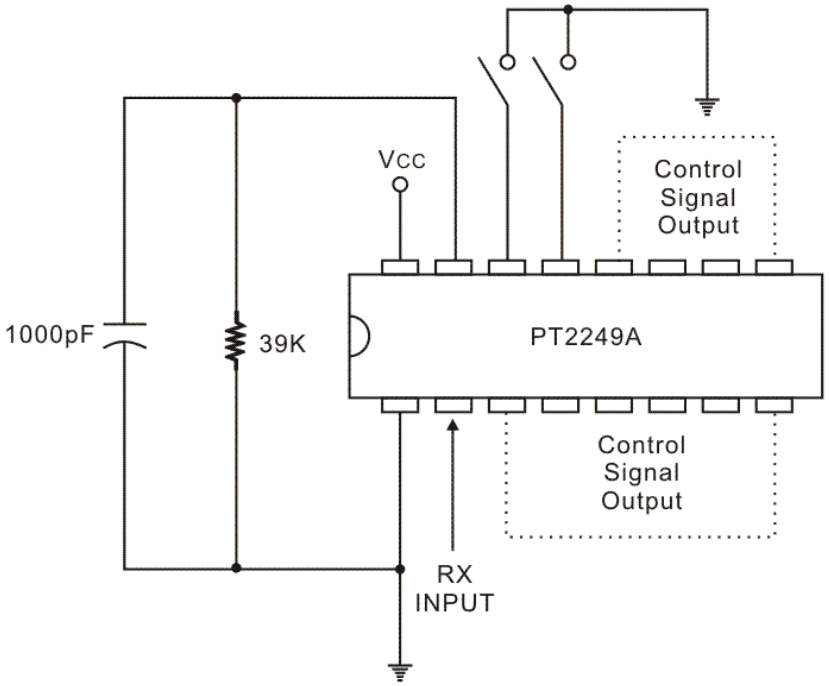
Note: Exceeding the maximum rating may cause permanent damage to devices.

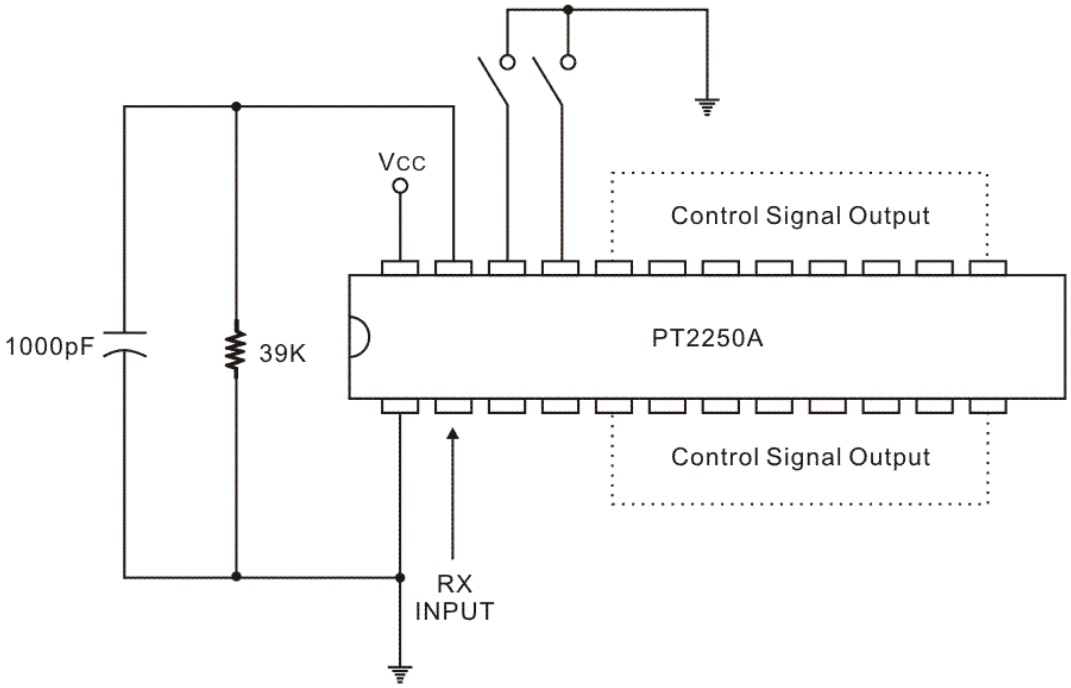
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=5V and Ta=25 ℃)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating supply voltage		Vcc	All Function Operations	2.3	-	5.0	V
Operating supply current		Icc	Key on without Load	-	-	1.0	mA
Oscillation frequency		fosc	Vcc=5 V	25	34	41	KHz
Output Current	"H" level	I_{OH}	Vo=4V	-1.0	-	-	mA
	"L" level	I_{OL}	Vo=1 V	1.0	-	-	mA
Pull-up resistor		Rup		150	300	450	KΩ
RXIN	Input current	I_{IH}	V_I=5V	-1.0	-	1.0	μA
	Input circuit threshold voltage	V_I		2.0	2.5	3.0	V
	Input hysterestic voltage	V_{HIS}		-	0.6	-	V
Stand-by current	PT2249/50A	I_{SB}	RXIN=0V OSC=5V (All Outputs floating)	-	-	200	μA
	PT2249AL			-	-	300	
	PT2249AHN			-	-	300	

APPLICATION CIRCUIT





APPLICATION NOTE:

1. Combination of PT2248/PT2249A Series Code Bits

a) PT2249A Series Code Bit C1 is internally pulled high and thereby set at a default value of "1". Thus, PT2248 Code Bit C1 must be set at "1".

b) PT2249A Series Code Bits C2 and C3 may be programmed as follows:
   1) "0", "0" (This combination is not available with TC9149.)
   2) "0", "1"
   3) "1", "0"
   4) "1", "1"

c) To set Code Bit to "1" on PT2248, diodes must be connected to Code Terminal from the T1 ~ T3 terminals.

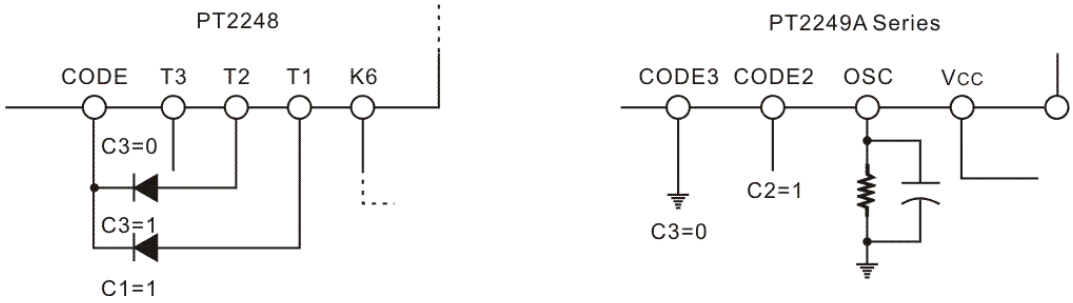
d) To set Code Bit to "0" on PT2248, the terminals must be kept floating, except C1 - add one diode.

e) The Code Bits Combinations of PT2248 and PT2249A Series are shown below:

PT2248			PT2249A Series	
C1	C2	C3	C2	C3
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

f) Example: (Refer to Example 1 diagram)

The following example shows the case when PT2248 Code Bits C1=1, C2=1, and C3=0. The CODE2 Pin of the PT2249A Series is programmed in floating state and CODE3 pin is connected to Vss (C2=1, C3=0.) In this way, the PT2249A Series can match the C2, C3 Code Bits of PT2248 and correctly decode the remote commands.



Example 1
Circuit Diagram when Code Bit C2 = 1 and C3 = 0

2. Combination of PT2248/PT2250A Series Code Bits

a) PT2250A Series Code Bit C3 is internally pulled high and thereby set at a default value of "1". Thus, PT2248 Code Bit C3 must be set at "1".

b) PT2250A Series Code Bits C2 and C3 may be programmed as follows:
1) "0", "0" (This combination is not available with TC9150.)
2) "0", "1"
3) "1", "0"
4) "1", "1"

c) To set Code Bit to "1" on PT2248, diodes must be connected to Code Terminal from the T1 ~ T3 terminals.

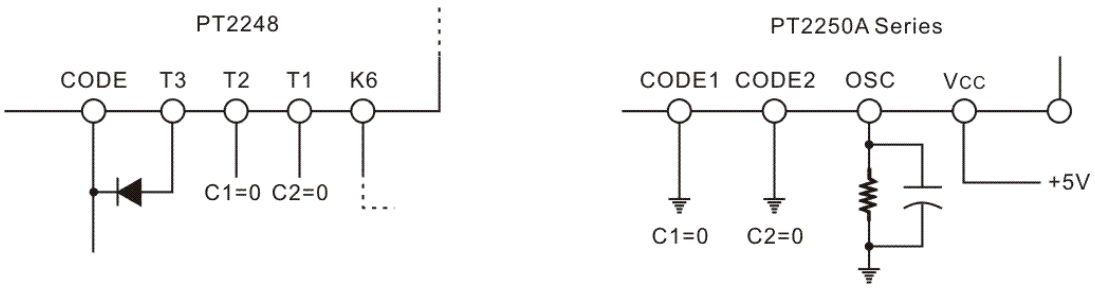
d) To set Code Bit to "0" on PT2248, the terminals must be kept floating.

e) The Code Bits Combinations of PT2248 and PT2250A Series are shown below:

PT2248			PT2250A Series	
C1	C2	C3	C1	C2
0	0	1	0	0
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1

f) Example: (Refer to Example 2 diagram)

The following example shows the case when PT2248 Code Bits C1=0, C2=0, and C3=1. The CODE1 and CODE2 pins of the PT2250A Series are connected to the V_{SS} (C1=0 and C2=0). In this way, the PT2250A or any of its series matches the C1 and C2 Code Bits of PT2248; thus, the remote commands are correctly decoded.



Example 2
Circuit Diagram when Code Bit C1=0 and C2=0

ORDER INFORMATION

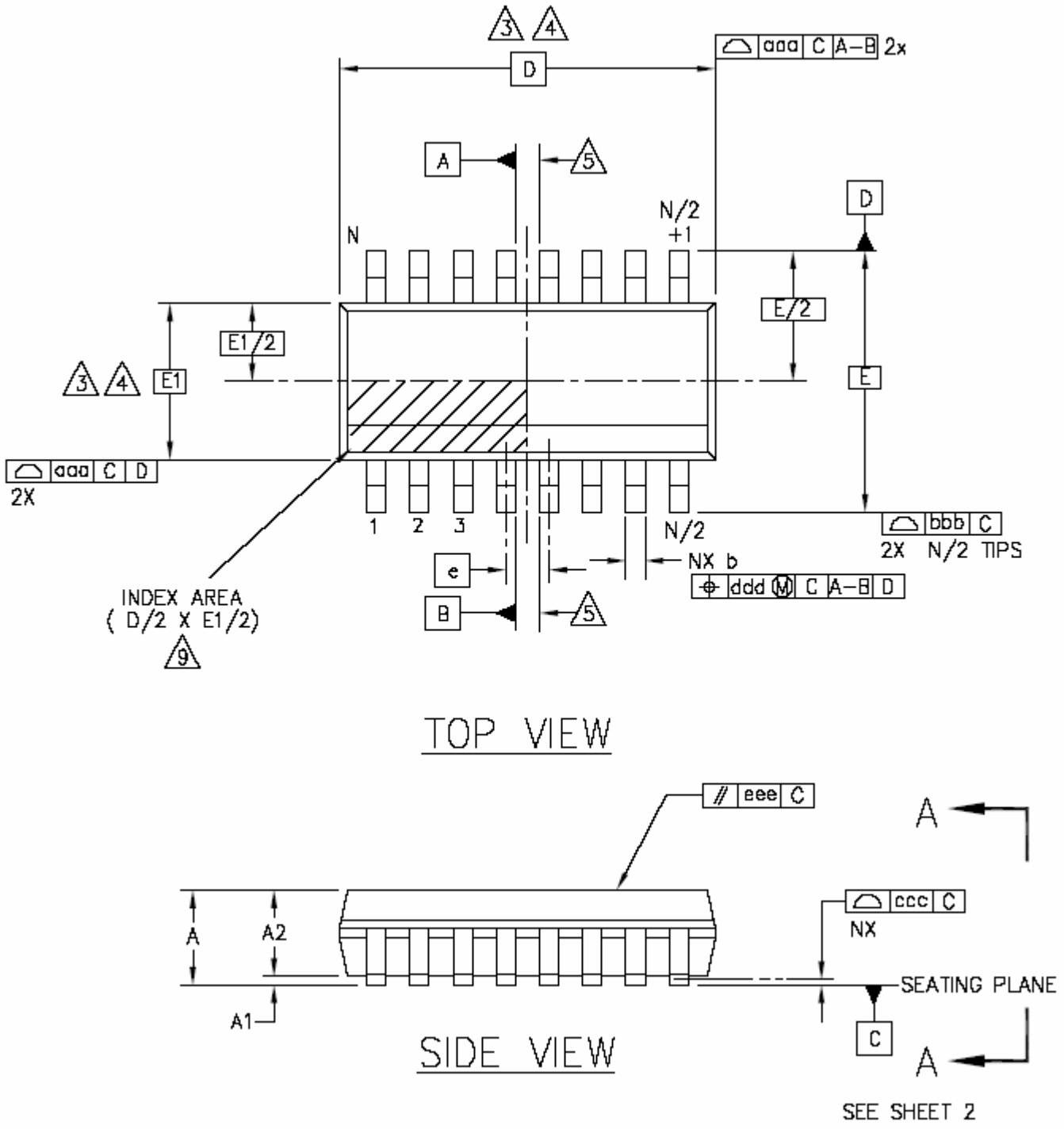
Valid Part Number	Package Type	Top Code
PT2249A	16 Pins, DIP, 300mil	PT2249A
PT2249AHN	16 Pins, DIP, 300mil	PT2249AHN
PT2249AL	16 Pins, DIP, 300mil	PT2249AL
PT2249A-SN	16 Pins, SOP, 150mil	PT2249A-SN
PT2250A	24 Pins, DIP, 600mil	PT2250A

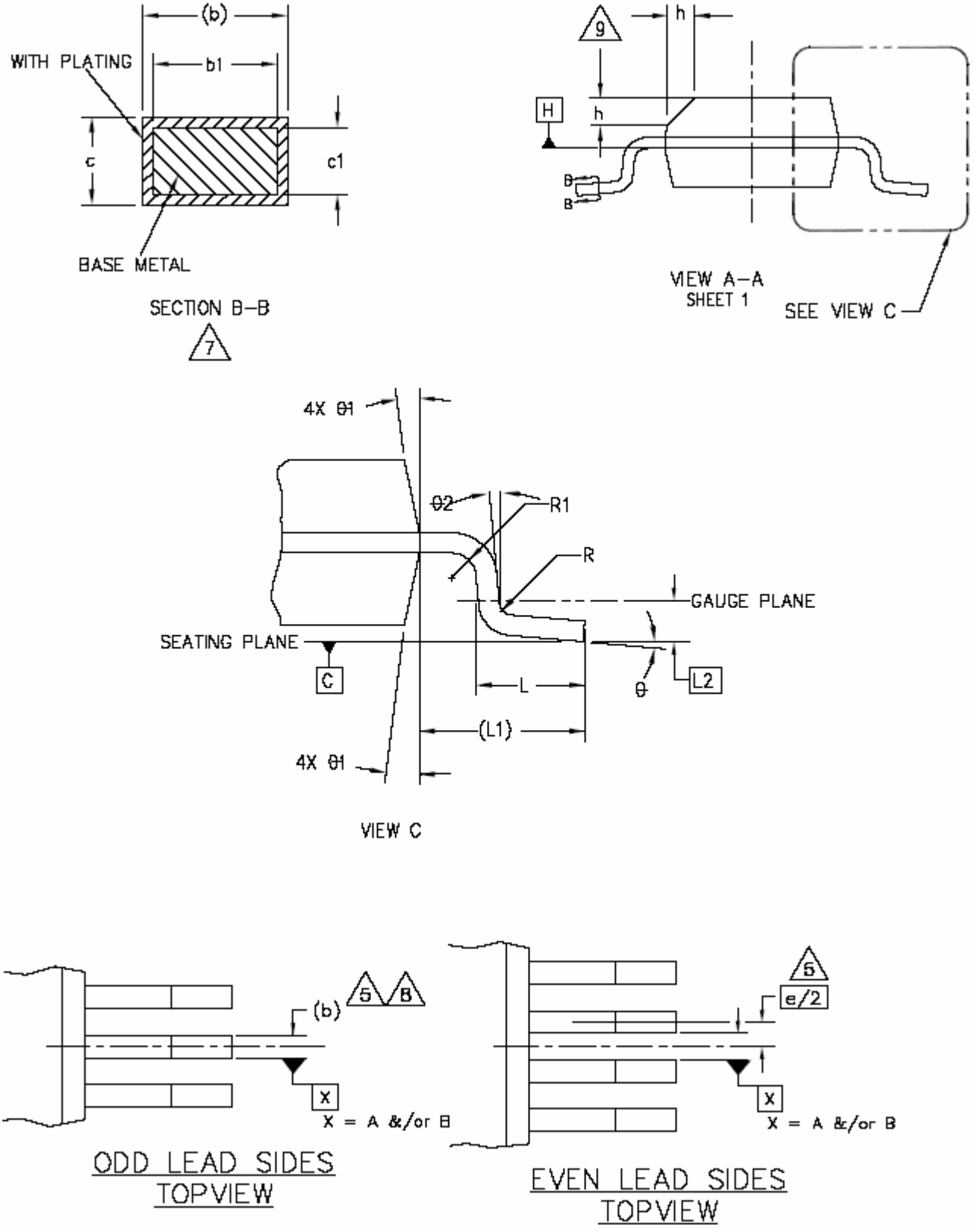
Functions:
1. A – Advanced Version
2. N – Inversed RXIN Input
3. L – Advanced Dependent Cyclic (Toggle) Outputs
4. H – Output Format same as “L”, except that when HP1 or HP2 is active, it will clear CP1.

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PACKAGE INFORMATION

16 PINS, SOP, 150 MIL



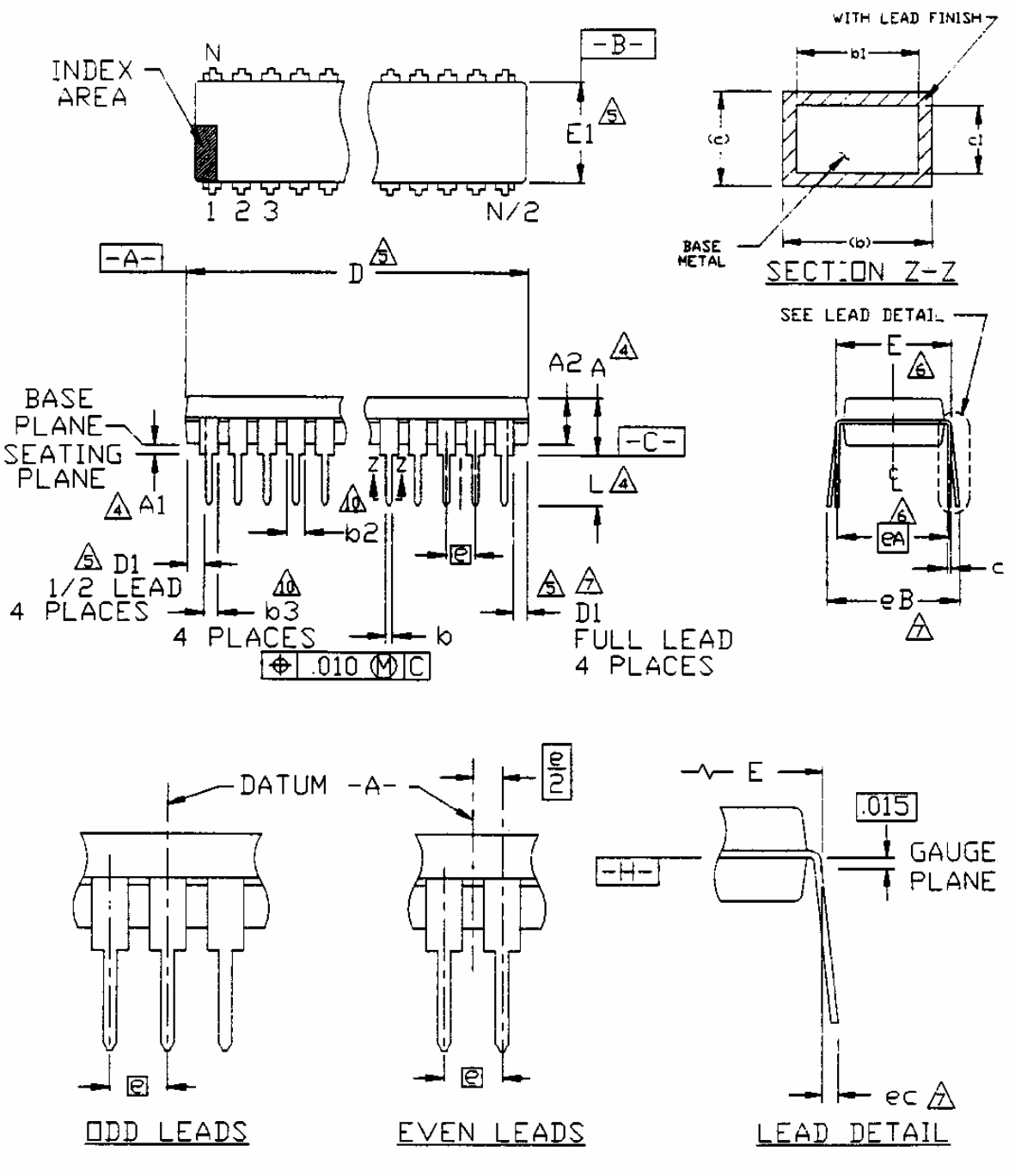

(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=16)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

16 PINS, DIP, 300 MIL



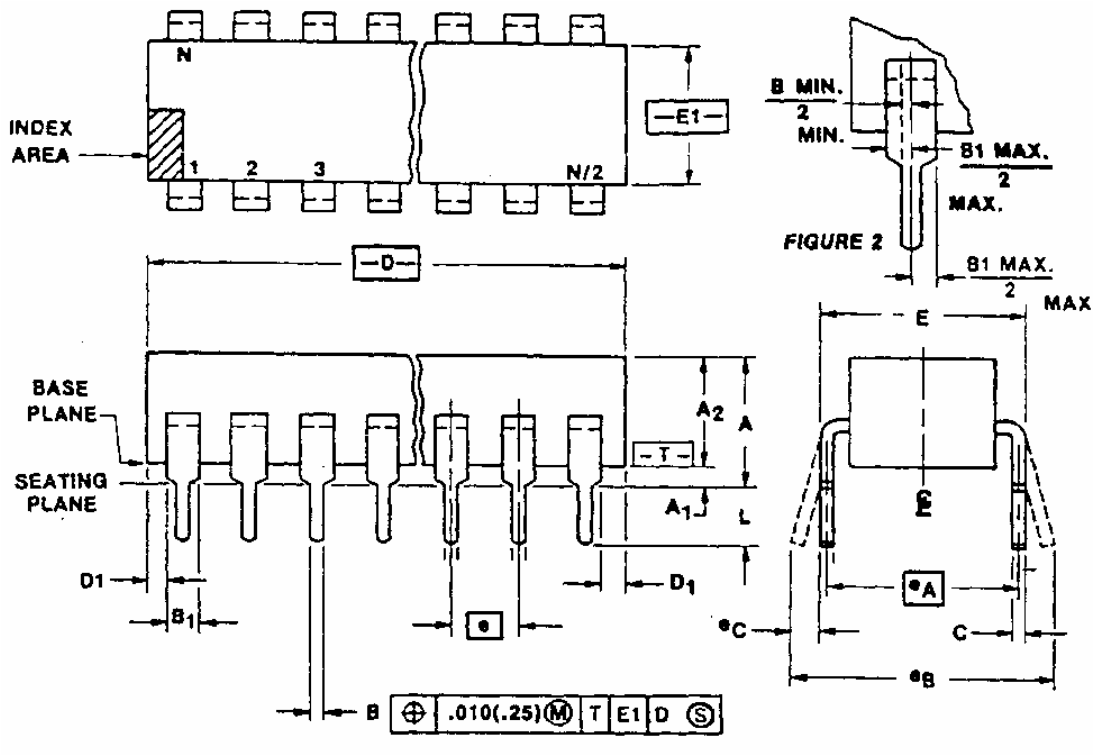
Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc	
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. Controlling Dimension: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. D, D1 and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and eA measured with the leads constrained to be perpendicular to datum -C-.
6. eB and eA are measured at the lead tips with the leads unconstrained.
7. N is the maximum number of terminal positions (N=16).
8. Pointed or rounded lead tips are preferred to ease insertion.
9. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25mm).
10. Variation AB is a full lead package.
11. Distance between leads including dambar protrusions to be 0.005 in minimum.
12. Datum plane -H- coincident with the bottom of lead where lead exits body.
13. Refer to JEDEC MS-001 Variation AB.

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24 PINS, DIP, 600 MIL



Symbol	Min.	Max.
A	-	0.250
A1	0.015	-
A2	0.125	0.195
B	0.014	0.022
B1	0.030	0.070
C	0.008	0.015
D	1.150	1.290
D1	0.005	-
E	0.600	0.625
E1	0.485	0.580
e	0.100 bsc	
eA	0.600 bsc	
eB	-	0.700
L	0.115	0.200

Notes:
1. Controlling Dimensions: INCH
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3
4. D and E1 dimensions, for ceramic packages, include allowance for glass overrun and meniscus and lid to base mismatch.
5. D and E1 dimensions for plastic packages, do not include mold, flash to protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm)
6. E and eA measured with the leads constrained to be perpendicular to plane T.
7. eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
8. N is the maximum number of terminal positions. (N=24).
9. Refer to JEDEC MS-011 Variation AA.

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