VITELIC

V61C35 FAMILY
HIGH PERFORMANCE LOW POWER
2K x 8 DUAL PORT MEMORY

Features

- 2K x 8 bit CMOS Static RAM with 3-state outputs
- High Speed Multiplexed Dual Port operation
  - 55ns, 70ns, 90ns, 120ns access time
- Battery backup 2 volt data retention
- Low power operation
  - Operating 200 mW (typ.)
  - Standby 15 μW (typ.)
- Full CMOS memory cell
- Both ports have full Read/Write capability
- VICMOS process virtually eliminates alpha particle induced soft errors
- All I/O is fully TTL compatible
- Single 5V power supply
- 48 pin DIP or 52 pin PLCC
- Pin compatible with V61C32 arbitrated dual port memory.

Description

The Vitelic V61C35 is a CMOS 2K x 8 low-cost dual port SRAM that eliminates on-chip arbitration to fit applications where timing or design makes arbitration unnecessary. By eliminating the ability to perform on-chip resolution of simultaneous access requests, the V61C35 can provide an extremely low-cost alternative to more expensive dual port RAM devices. Fabrication with the VICMOS technology provides a high performance, low power alternative to NMOS memory.

The Vitelic V61C35 provides two parallel 8-bit ports with separate controls, addresses, and I/O, permitting read or write access to any memory location. When a port is inactive and $\overline{CE}$ is "high", automatic power-down circuitry places it in the Standby Mode to reduce overall power dissipation.

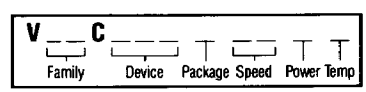
The Vitelic V61C35 offers a battery backup Data Retention Mode that allows the device power dissipation to be reduced to only 2.5 μW when operating from a 2 volt source.

The Vitelic V61C35 comes in a 48 pin DIP package for insertion into mounting holes on 600 mil (15.2 mm) centers, or 52 pin PLCC.

Device Usage Chart

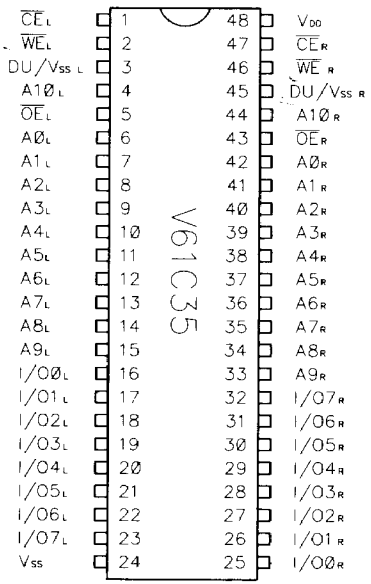
Operating Temperature Range	Package Outline				Access Time (ns)				Power		Temperature Mark
	P	C	G	J	55	70	90	120	Low	Std.	
0°C to 70°C	•			•	•	•	•		•	•	Blank
-40°C to +85°C	•	•	•	•		•	•	•	•	•	I
-55°C to +125°C		•	•			•	•	•	•	•	X

Package	Std.	Pin Count
Plastic DIP	P	48
PLCC (J Lead)	J	52
Ceramic Side Brazed	C	48
Ceramic LCC	G	48



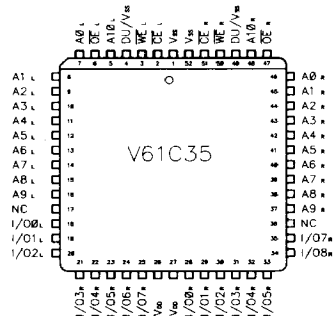
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DIP PIN CONFIGURATION
Top View



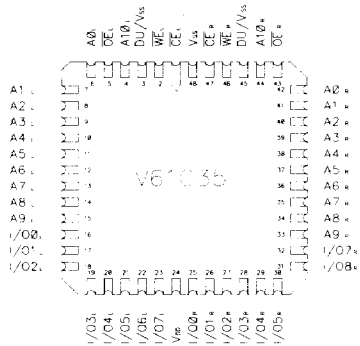
NOTE: For lowest power dissipation, pins 3 & 45 should be connected to V_{SS}. Otherwise, no connection should be made.

PLCC PIN CONFIGURATION
Top View

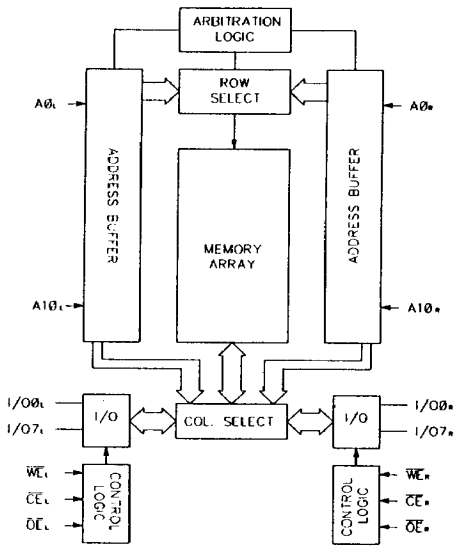


NOTE: V_{DD} must be applied to both pins 1 and 52. V_{SS} must be applied to both pins 26 and 27. For lowest power dissipation, pins 4 and 49 should be connected to V_{SS}. Otherwise, no connection should be made.

LCC PIN CONFIGURATION
Top View



BLOCK DIAGRAM



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Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Voltage on any Pin with Respect to V_{SS}	−0.5* to +7.0	V
T_A	Operating Temperature Under Bias	Same as Recommended Operating Conditons	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

*−3.5V for 20 ns pulse.

NOTE:
1. Operation at or near absolute maximum ratings can affect device reliability.

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{OUT}	Output Capacitance	V_{IN} = 0V	5	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	5	pF

Recommended Operating Conditions

T_A = Operating Temperature Range

Range	Temperature
Commercial	0°C to 70°C
Industrial	−40°C to +95°C
Extended	−55°C to +125°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0.0	0.0	0.0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{DD}	V
V_{IL}	Input Low Voltage	−0.5*	—	+0.8	V

*−3.5V for 20 ns pulse.

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Read-Write Control

Left Port Inputs			Right Port Inputs			Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	
X	H	X	X	X	X	Left Port in Power Down Mode
X	X	X	X	H	X	Right Port in Power Down
L	L	X	X	X	X	Data on Left Port Written Into Memory
H	L	L	X	X	X	Data in Memory Output on Left Port
X	X	X	L	L	X	Data on Right Port Written Into Memory
X	X	X	H	L	L	Data in Memory Output on Right Port

H = High, L = Low, X = Don't Care

DC Characteristics

For operating conditions, refer to temperature range marking

Symbol	Parameter	Test Conditions	Range	V61C35			V61C35L			Unit
				Min.	Typ. (1)	Max.	Min.	Typ. (1)	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = 5.5V, 0.0V ≤ V_{IN} ≤ V_{DD}	*—	—	—	10	—	—	5	µA
			**I	—	—	10	—	—	5	
			***X	—	—	20	—	—	10	
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ ≥ V_{IH}, 0.0V ≤ V_{OUT} ≤ V_{DD}	—	—	—	10	—	—	5	µA
			I	—	—	10	—	—	5	
			X	—	—	20	—	—	10	
V_{IH}	Input High Voltage			2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage			0.5 (2)	—	+0.8	-0.5 (2)	—	+0.8	V
I_{DD1}	TTL Operating Current (One Port Active)	$\overline{CE}_L$ or $\overline{CE}_R$ ≤ V_{IL}, Other $\overline{CE}$ ≥ V_{IH}, Active Port Outputs Open		—	40	110	—	40	75	mA
I_{DD2}	CMOS Operating Current (One Port Active)	$\overline{CE}_L$ or $\overline{CE}_R$ ≤ V_{SS} +0.2V Other $\overline{CE}$ ≥ V_{DD} -0.2V V_{SS} +0.2V ≥ V_{IN} ≥ V_{DD} -0.2V Active Port Outputs Open		—	40	90	—	35	65	mA
I_{SB1}	TTL Standby Current (Both Ports TTL Standby)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}		—	15	50	—	15	30	mA
I_{SB2}	CMOS Standby Current (Both Ports CMOS Standby	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} -0.2V V_{SS} +0.2V ≥ V_{IN} ≥ V_{DD} -0.2V	—	—	5	10000	—	3	100	µA
			I	—	5	15000	—	3	250	
			X	—	5	15000	—	3	4000	
V_{OL}	Output Low Voltage	I_{OL} = 3.5 mA		—	—	0.4	—	—	0.4	V
		I_{OL} = 8.0 mA		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4	—	—	2.4	—	—	V

NOTES:

1. V_{DD} = 5.0V, T_A = +25°C.
2. V_{IL} (min) = -3.5V for pulse width less than 20 ns.

* (—) T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

** (I) T_A = -40°C to +85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

*** (X) T_A = -55°C to +125°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise noted

For availability in a particular temperature range, refer to Device Usage Chart, Page 85

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AC Characteristics

For operating conditions refer to Temperature Range Marking

Read Cycle

Symbol	Parameter	Range	55		70		90		120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time		55	—	70	—	90	—	120	—	ns
t_{AA}	Address Access Time		—	55	—	70	—	90	—	120	ns
t_{ACE}	Chip Enable Access Time		—	55	—	70	—	90	—	120	ns
t_{AOE}	Output Enable Access Time		—	20	—	35	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	*—	10	—	10	—	10	—	—	—	ns
		**I	—	—	10	—	10	—	20	—	
		***X	—	—	10	—	15	—	20	—	
t_{LZ}	Output Low-Z Time (1)		5	—	5	—	5	—	10	—	ns
t_{HZ}	Output High-Z Time (1)		--	20	—	35	—	40	—	40	ns
t_{PU}	$\overline{CE}$ to Power Up Time		0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time		—	35	—	40	—	50	—	50	ns

Write Cycle

Symbol	Parameter	Range	55		70		90		120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		55	—	70	—	90	—	120	—	ns
t_{EW}	Chip Enable to End of Write		50	—	65	—	85	—	110	—	ns
t_{AW}	Address Valid to End of Write		50	—	65	—	85	—	110	—	ns
t_{AS}	Address Setup Time		0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	—	40	—	50	—	60	—	—	—	ns
		I	—	—	50	—	60	—	90	—	
		X	—	—	55	—	60	—	90	—	
t_{WR}	Write Recovery Time		5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	—	30	—	40	—	40	—	—	—	ns
		I	—	—	40	—	50	—	70	—	
		X	—	—	40	—	50	—	70	—	
t_{DH}	Data Hold Time		0	—	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time (1)		—	20	—	35	—	40	—	50	ns
t_{WZ}	$\overline{WE}$ to Output High-Z (1)		0	25	0	35	0	40	0	50	ns
t_{OW}	Output Active From End of Write (1)		0	—	0	—	0	—	0	—	ns

NOTE:

1. Transition is measured ± 500 mV from low or high voltage with load (Figure 2). This parameter is sampled and not 100% tested.

* (—) T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

** (I) T_A = –40°C to + 85°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

*** (X) T_A = –55°C to + 125°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise noted

For availabillity in a particular temperature range, refer to Device Usage Chart, Page 85

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AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

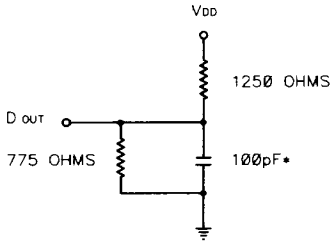


Figure 1.
*Including scope and jig.

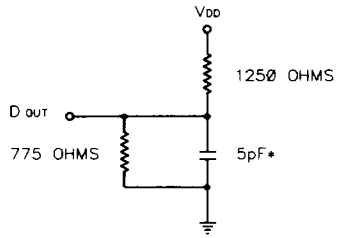
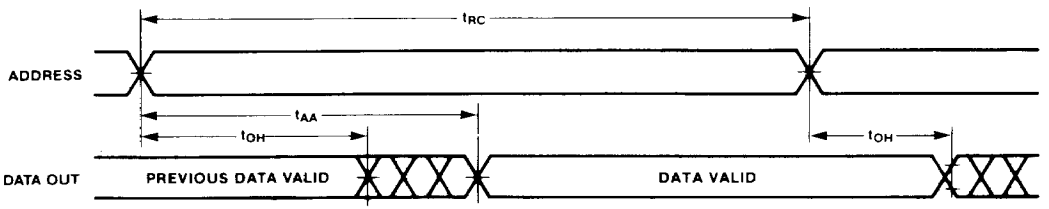
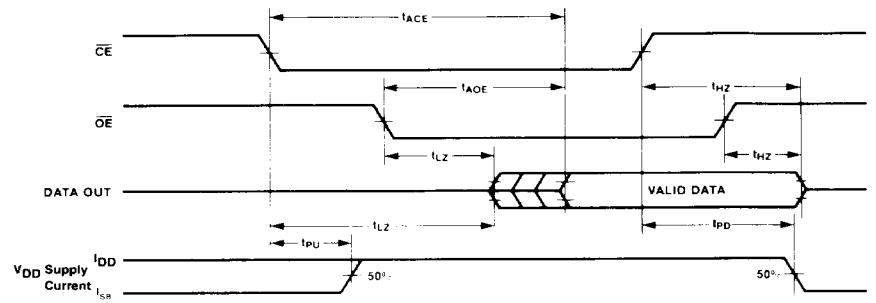


Figure 2.
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

Timing Waveform of Read Cycle No. 1 Either Side (1, 2, 5)

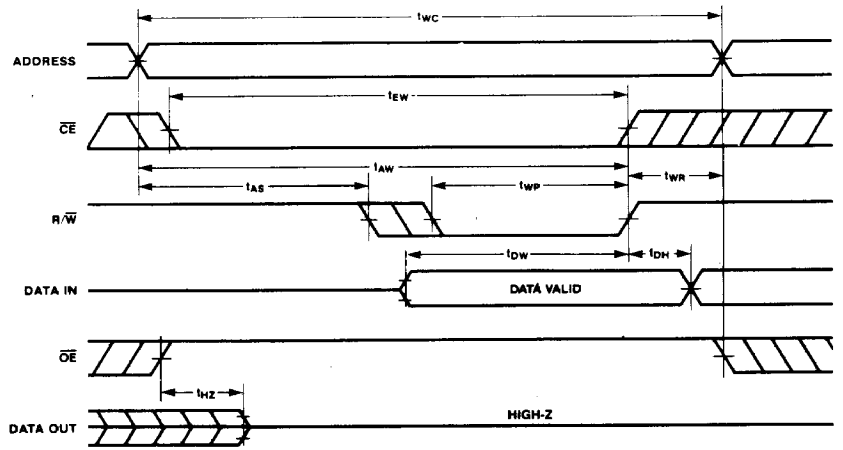


Timing Waveform of Read Cycle No. 2 Either Side (1, 3)

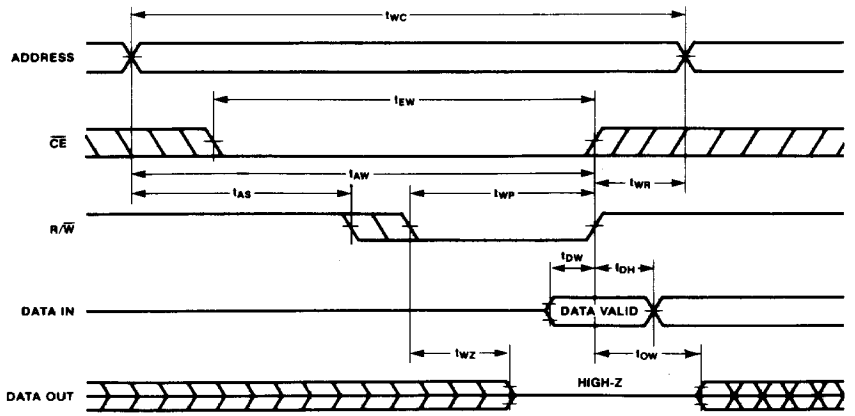


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Timing Waveform of Write Cycle No. 2 Either Side (4, 6)



Timing Waveform of Write Cycle No. 1 Either Side (4, 6)



NOTES:

1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{OE}$ = V_{IL}.
6. R/$\overline{W}$ = V_{IH} during address transition.

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Data Retention Characteristics

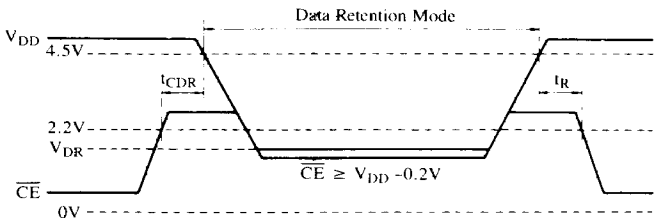
V61C35L

Symbol	Parameter	Test Conditions	Min.	Typ. (1)	Max.	Unit
V_{DR}	V_{DD} for Retention Data	V_{DD} = 3.0V, $\overline{CE} \geq V_{DD}$ = 3.0V $V_{IN} \geq V_{DD}$ −0.2V or $V_{IN} \leq$ +0.2V	2.0	—	—	V
I_{DDDR}	Data Retention Current		—	3	100 (3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t_R	Operation Recovery Time		t_{RC} (2)	—	—	ns

NOTES:

1. V_{DD} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. 100 µA max. for 0°C to 70°C, 250 µA max. for −40°C to +85°C, 4000 µA max. for −55°C to +125°C.

Low V_{DD} Data Retention Waveform

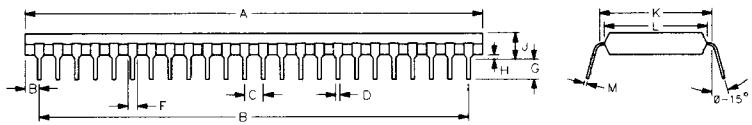


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Package Outline

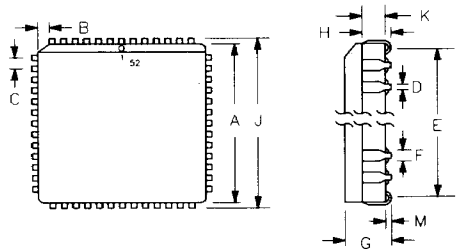
48 Pin Plastic

Dimension	Inches	Millimeters
A	2.460 max.	62.484 max.
B	.080	2.032
C	.1	2.54
D	.015/.020	.381/.508
E	2.3	58.42
F	.040/.065	1.016/1.651
G	.125/.160	3.175/4.064
H	.015/.065	.381/1.651
J	.160/.225	4.064/5.715
K	.590/.610	14.986/15.494
L	.530/.550	13.462/13.970
M	.009/.012	.229/.305



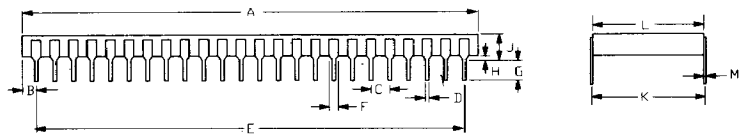
52 Pin PLCC-J

Dimension	Inches	Millimeters
A	.760 max.	19.30 max.
B	.045	1.14
C	.050 typ.	1.27 typ.
D	.017 typ.	.43 typ.
E	.730 max.	18.54 max.
F	.026/.032	.66/.81
G	.180 max.	4.57
H	.098 nom.	2.49
J	.795	20.19
K	.055 nom.	1.40
M	.030/0.40	.76/1.14



48 Pin Ceramic

Dimension	Inches	Millimeters
A	2.430 max.	61.722 max.
B	.065	1.651
C	.100	2.54
D	.015/.023	.381/.584
E	2.300	58.42
F	.038/.060	.965/1.524
G	.120/.160	3.048/4.064
H	.030/.070	0.762/1.778
J	.100/.200	2.54/5.08
K	.590/.620	14.986/15.748
L	.550/.610	13.97/15.494
M	.008/.012	.203/.305



48 Pin CLCC

Dimension	Inches	Millimeters
A	.554/.572	14.072/14.529
B	.045/.055	1.143/1.397
C	.037/.043	.94/1.092
D	.015/.025	.381/.635
E	.434/.446	11.024/11.328
J	.065/.125	1.651/3.175

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