PRELIMINARY

CYM74B430
CYM74P430/31
CYM74S430/31

Intel® 82340FX PCIset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family that adheres to the Intel COAST 1.1 specification**
- **Asynchronous (CYM74B430), synchronous pipelined (CYM74P430, CYM74P431), or synchronous (CYM74S430, CYM74S431) configurations with presence and configuration detect pins**
- **Ideal for Intel® P54C-based systems with the 82430FX (Triton) chipset**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector•3.3V compatible inputs/data outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chipset.

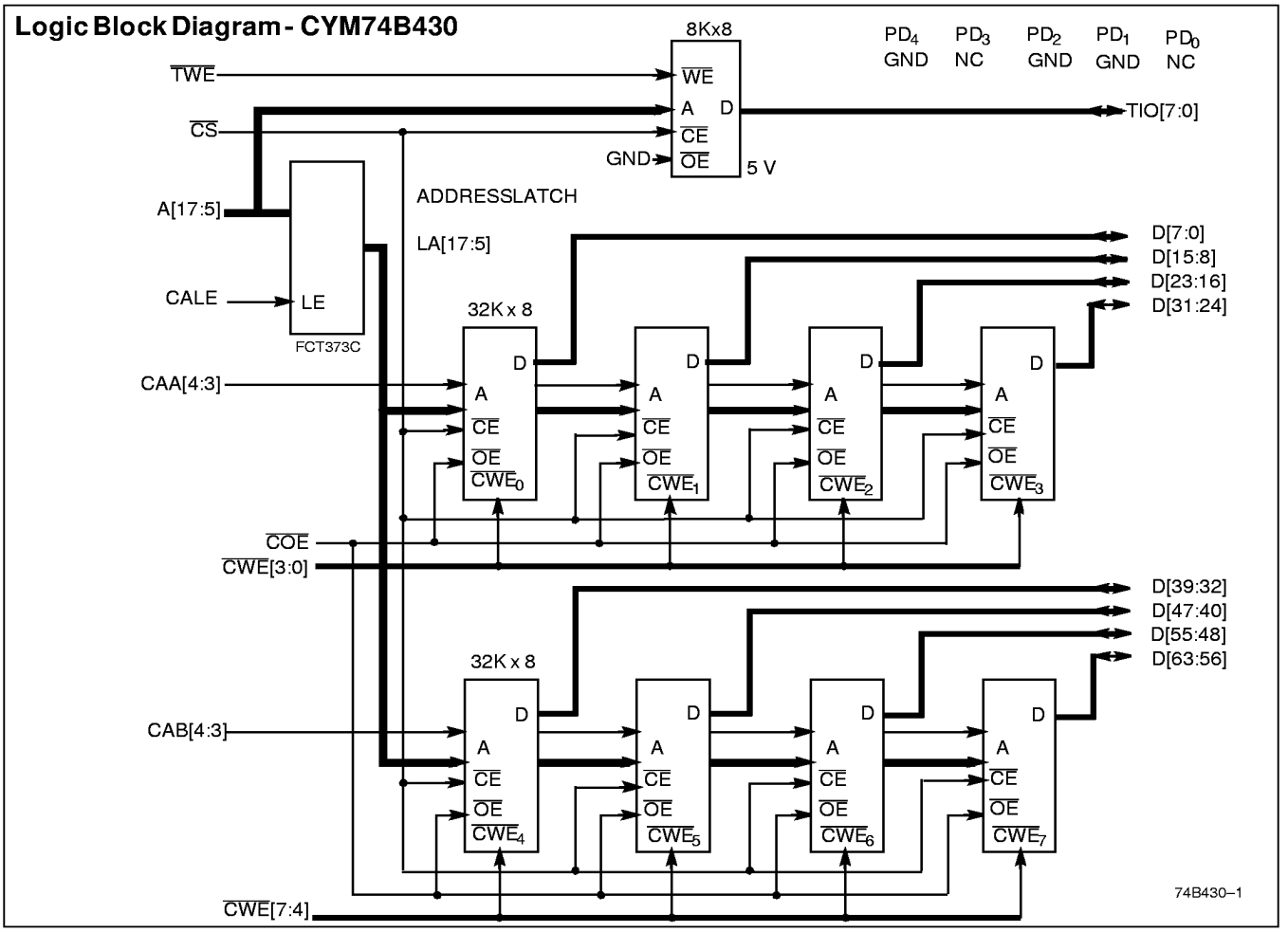
CYM74B430 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution with industry standard 32Kx8 5V SRAMs and 3.3V level translators. The CYM74B430 is organized as 32K by 64-bits with an 8Kx8 tag that supports 3-2-2-2 read and 4-2-2-2 write cycles at CPU bus speeds up to 66 MHz.

The synchronous modules are available with low cost synchronous pipelined RAMs, or high performance synchronous burst RAMs. The synchronous pipelined modules are based on a 16Kx64 RAM. The CYM74P430 is a 256-KB module while the CYM74P431 is a 512-KB module.

The CYM74S430 and CYM74S431 are high performance synchronous burst cache modules that provide 256 KB and 512 KB of cache respectively. The modules support 3-1-1-1 performance at 66 MHz. Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram - CYM74B430

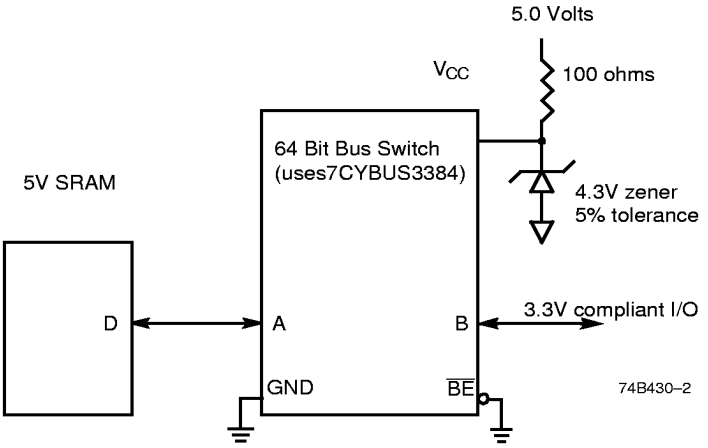


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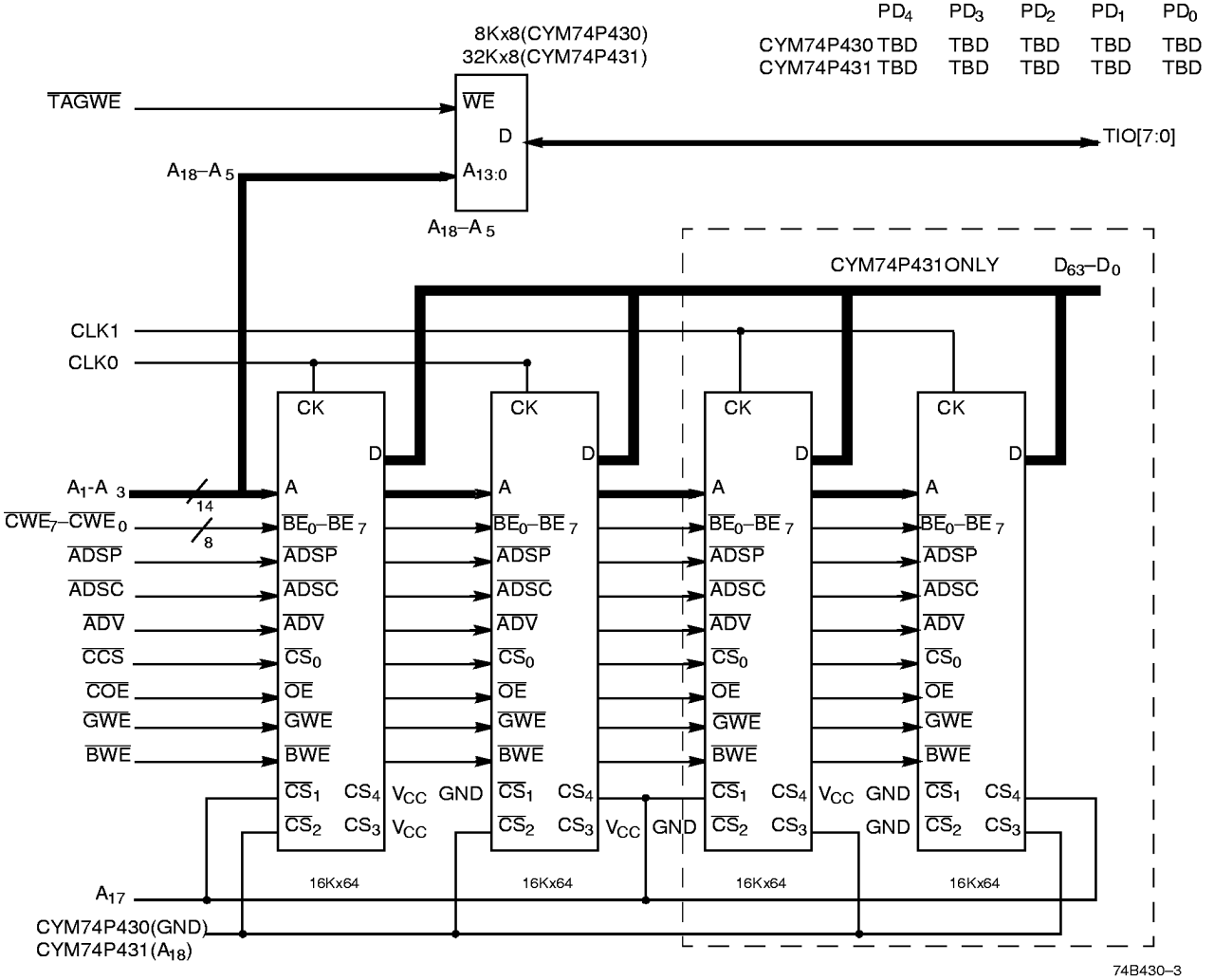
December 1994 – Revised October 1995

Block Diagram: 5V to 3.3V Level Conversion (CYM74B430)



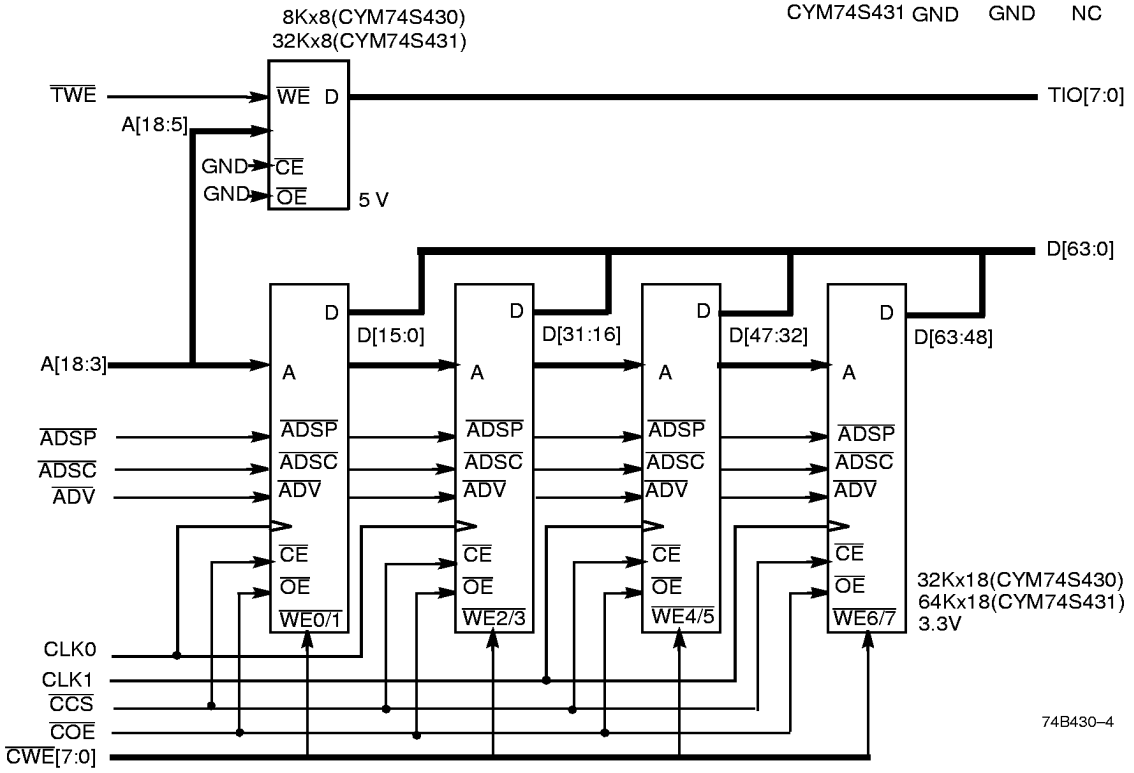
Logic Block Diagram - CYM74P430, CYM74P431

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM74P430	TBD	TBD	TBD	TBD	TBD
CYM74P431	TBD	TBD	TBD	TBD	TBD



Logic Block Diagram - CYM74S430/CYM74S431[1]

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM74S430	GND	NC	GND	NC	GND
CYM74S431	GND	GND	NC	NC	GND



Note:

1. A18 is not used by CYM74S430. DP pins are pulled high through 10KΩ.

Selection Guide

	Asynchronous Cache Modules		
Part Number	**74B430-50**	**74B430-60**	**74B430-66**
Cache Size	256 KB		
System Clock (MHz)	50	60	66
Data t_{AA}	20 ns	17 ns	15 ns
Tag t_{AA}	30 ns	20 ns	15 ns

	Synchronous Pipelined Cache Modules					
Part Number	**74P430-50**	**74P430-60**	**74P430-66**	**74P431-50**	**74P431-60**	**74P431-66**
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{CDV}	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

	Synchronous Burst Cache Modules					
Part Number	**74S430-50**	**74S430-60**	**74S430-66**	**74S431-50**	**74S431-60**	**74S431-66**
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{CDV}	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

PinConfiguration

Dual Read–Out SIMM (DIMM)
Top View

GND	81	1	GND	
TIO_1	82	2	TIO_0	
TIO_7	83	3	TIO_2	
TIO_5	84	4	TIO_6	
TIO_3	85	5	TIO_4	
RSVD	86	6	RSVD	
V_{CC}	87	7	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
RSVD	88	8	$\overline{TWE}$	
(CYM74P43X,CYM74S43x) $\overline{ADV}$ / (CYM74B430) CAA_4	89	9	CAA_5 (CYM74B430) / $\overline{ADSC}$ (CYM74P43X,CYM74S43X)	
GND	90	10	GND	
$\overline{COE}$	91	11	$\overline{CWE_4}$	
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	
V_{CC}	95	15	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
$\overline{CWE_3}$	96	16	CAB_4 (CYM74B430) / $\overline{CCS}$ (CYM74P43X,CYM74S43X)	
(CYM74P43X,CYM74S43x) NC / (CYM74B430) CAB_3	97	17	($\overline{GWE}$) (CYM74P43X	
(CYM74P43X,CYM74S43x) NC / (CYM74B430) CALE	98	18	($\overline{BWE}$) (CYM74P43X)	
GND	99	19	GND	
RSVD	100	20	A_3	
A_4	101	21	A_7	
A_6	102	22	A_5	
A_8	103	23	A_{11}	
A_{10}	104	24	A_{16}	
V_{CC}	105	25	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
A_{17}	106	26	NC (74B430, 74S430) / GND (74P430) / A_{18} (74P431, 74S431)	
GND	107	27	GND	
A_9	108	28	A_{12}	
A_{14}	109	29	A_{13}	
A_{15}	110	30	NC (CYM74B430) / $\overline{ADSP}$ (CYM74P43X,CYM74S43X)	
RSVD	111	31	$\overline{CS}$ (CYM74B430) / NC (CYM74P43X,CYM74S43X)	
PD_0	112	32	NC ($\overline{ECS2}$)	
PD_2	113	33	PD_1	
PD_4	114	34	PD_3	
GND	115	35	GND	
(CYM74P43X,CYM74S43x) CLK_0 / (CYM74B430) NC	116	36	NC (CYM74B430, CYM74P430) / CLK_1 (CYM74P431,CYM74S43X)	
GND	117	37	GND	
D_{63}	118	38	D_{62}	
V_{CC}	119	39	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
D_{61}	120	40	D_{60}	
D_{59}	121	41	D_{58}	
D_{57}	122	42	D_{56}	
GND	123	43	GND	
D_{55}	124	44	D_{54}	
D_{53}	125	45	D_{52}	
D_{51}	126	46	D_{50}	
D_{49}	127	47	D_{48}	
GND	128	48	GND	
D_{47}	129	49	D_{46}	
D_{45}	130	50	D_{44}	
D_{43}	131	51	D_{42}	
V_{CC}	132	52	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
D_{41}	133	53	D_{40}	
D_{39}	134	54	D_{38}	
D_{37}	135	55	D_{36}	
GND	136	56	GND	
D_{35}	137	57	D_{34}	
D_{33}	138	58	D_{32}	
D_{31}	139	59	D_{30}	
V_{CC}	140	60	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
D_{29}	141	61	D_{28}	
D_{27}	142	62	D_{26}	
D_{25}	143	63	D_{24}	
GND	144	64	GND	
D_{23}	145	65	D_{22}	
D_{21}	146	66	D_{20}	
D_{19}	147	67	D_{18}	
V_{CC}	148	68	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
D_{17}	149	69	D_{16}	
D_{15}	150	70	D_{14}	
D_{13}	151	71	D_{12}	
GND	152	72	GND	
D_{11}	153	73	D_{10}	
D_9	154	74	D_8	
D_7	155	75	D_6	
V_{CC}	156	76	NC (CYM74B430) / V_{CCQ} (CYM74P43X,CYM74S43X)	
D_5	157	77	D_4	
D_3	158	78	D_2	
D_1	159	79	D_0	
GND	160	80	GND	

74B430–5

Pin Definitions

Common Signals	Description
V_{CC}	5V Supply
GND	Ground
A[18:3]	Addresses from processor
$\overline{COE}$	Output Enable
$\overline{CWE}$[7:0]	Byte Write Enables
PD_0-PD_4	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
$\overline{TWE}$	Tag Write Enable signal
NC	Signal not connected on module
RSVD	Reserved
CYM74B430 Only Signals	**Description**
CAA[4:3]	Lower two address bits for bank 0
CAB[4:3]	Lower two address bits for bank 1
CALE	Latch Enable
$\overline{CS}$	Chip Select
CYM74P43X, CYM74S43X Signals	**Description**
V_{CCQ}	3.3V Supply
$\overline{ADSP}$	Processor Address Strobe
$\overline{ADSC}$	Cache Controller Address Strobe
$\overline{ADV}$	Burst Address Advance
$\overline{CCS}$	Chip Select
CLK[1:0]	Clock signals, CLK1 not used on CYM74P430

Presence Detect Pins

	PD_4	PD_3	PD_2	PD_1	PD_0
Asynchronous - CYM74B430	GND	NC	GND	GND	NC
Synchronous Pipelined - CYM74P430	TBD	TBD	TBD	TBD	TBD
Synchronous Pipelined - CYM74P431	TBD	TBD	TBD	TBD	TBD
Synchronous Burst - CYM74S430	GND	NC	GND	NC	GND
Synchronous Burst - CYM74S431	GND	GND	NC	NC	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential.... –0.5V to +5.25V

5V Supply Voltage to Ground Potential..... –0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +4.6V

DC Input Voltage..... –0.5V to +4.6V

Output Current into Outputs (LOW) .....20 mA

Operating Range

Range	Ambient Temperature	V_{CC}	V_{CCQ}
Commercial (CYM74B430)	0°C to +70°C	5V ± 5%	N/A
Commercial (CYM74P43X, CYM74S43X)	0°C to +70°C	5V ± 5%	5V ± 5% 3.3V+ 10% – 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	CYM74B430	–0.5	0.8	V
V_{IL}	Input LOW Voltage	CYM74P43X, CYM74S43X	–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = –4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74B430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1600	mA
I_{CC} (74P430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD	mA
I_{CC} (74P431)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD	mA
I_{CC} (74S430)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1200	mA
I_{CC} (74S431)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1400	mA

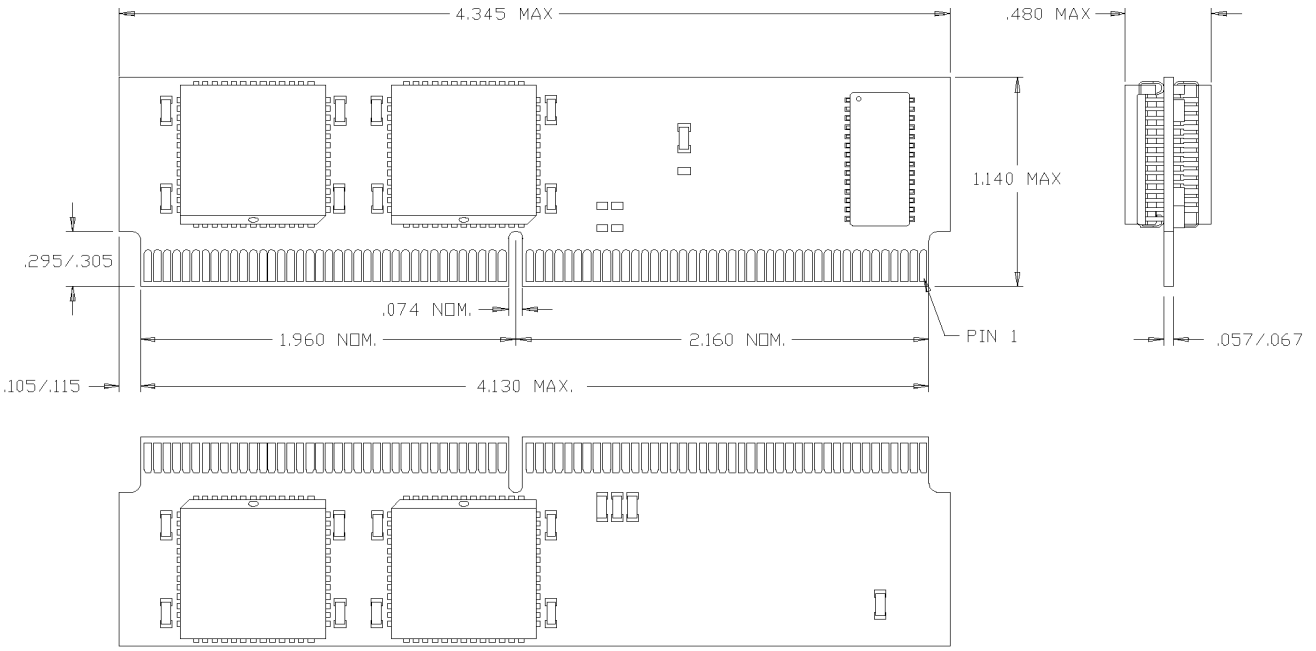
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74B430PM-50C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-50C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-50C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-50C	PM28		Sync Burst 256 KB	
	CYM74S431PM-50C	PM28		Sync Burst 512 KB	
60	CYM74B430PM-60C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-60C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-60C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-60C	PM28		Sync Burst 256 KB	
	CYM74S431PM-60C	PM28		Sync Burst 512 KB	
66	CYM74B430PM-66C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-66C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-66C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-66C	PM28		Sync Burst 256 KB	
	CYM74S431PM-66C	PM28		Sync Burst 512 KB	

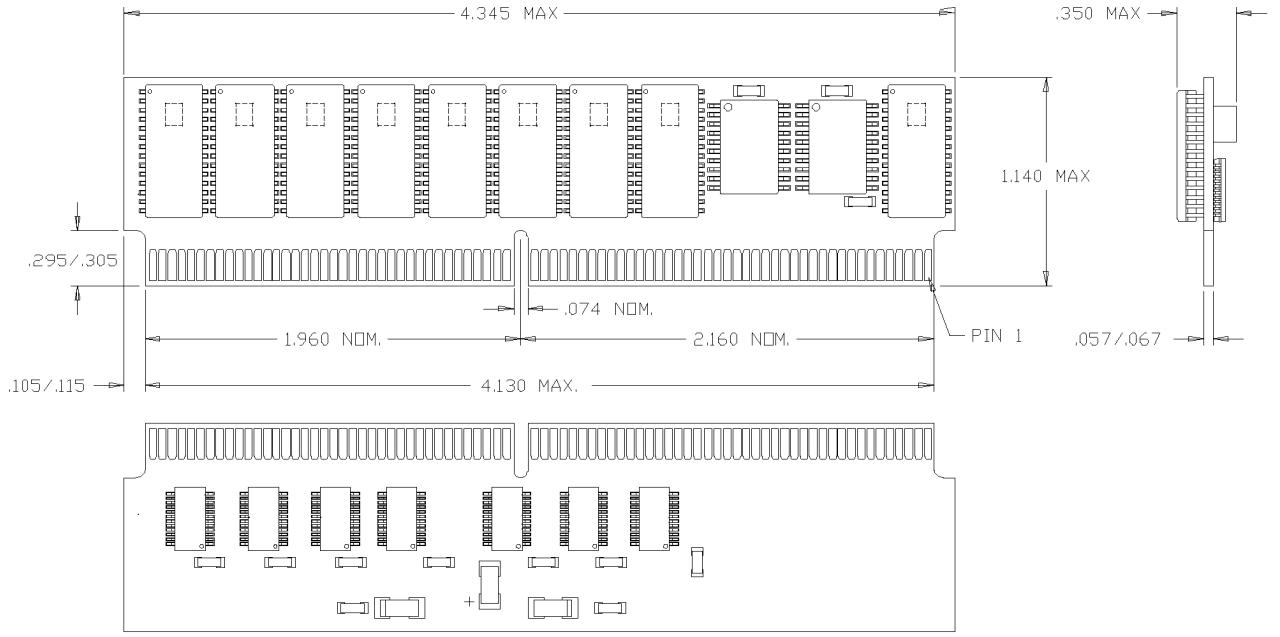
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Package Diagrams

160–Pin Dual Readout SIMM PM28



160–Pin Dual Readout SIMM PM34



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