Document Title

256K X 32Bit X 2 Banks Synchronous Graphic RAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	August 21, 2001	Preliminary
0.1	Update AC and DC data specification	October 22, 2001	
1.0	Final version release	September 29, 2003	Final
1.1	Add Pb-Free package type	August 19, 2004	

256K X 32 Bit X 2 Banks Synchronous Graphic RAM

Features

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks / Pulse $\overline{\text{RAS}}$
- MRS cycle with address key programs
  - CAS Latency (2,3)
  - Burst Length (1,2,4,8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM 0-3 for byte masking
- Auto & self refresh
- 32ms refresh period (2K cycle)

- 100 Pin QFP, LQFP (14 X 20 mm)

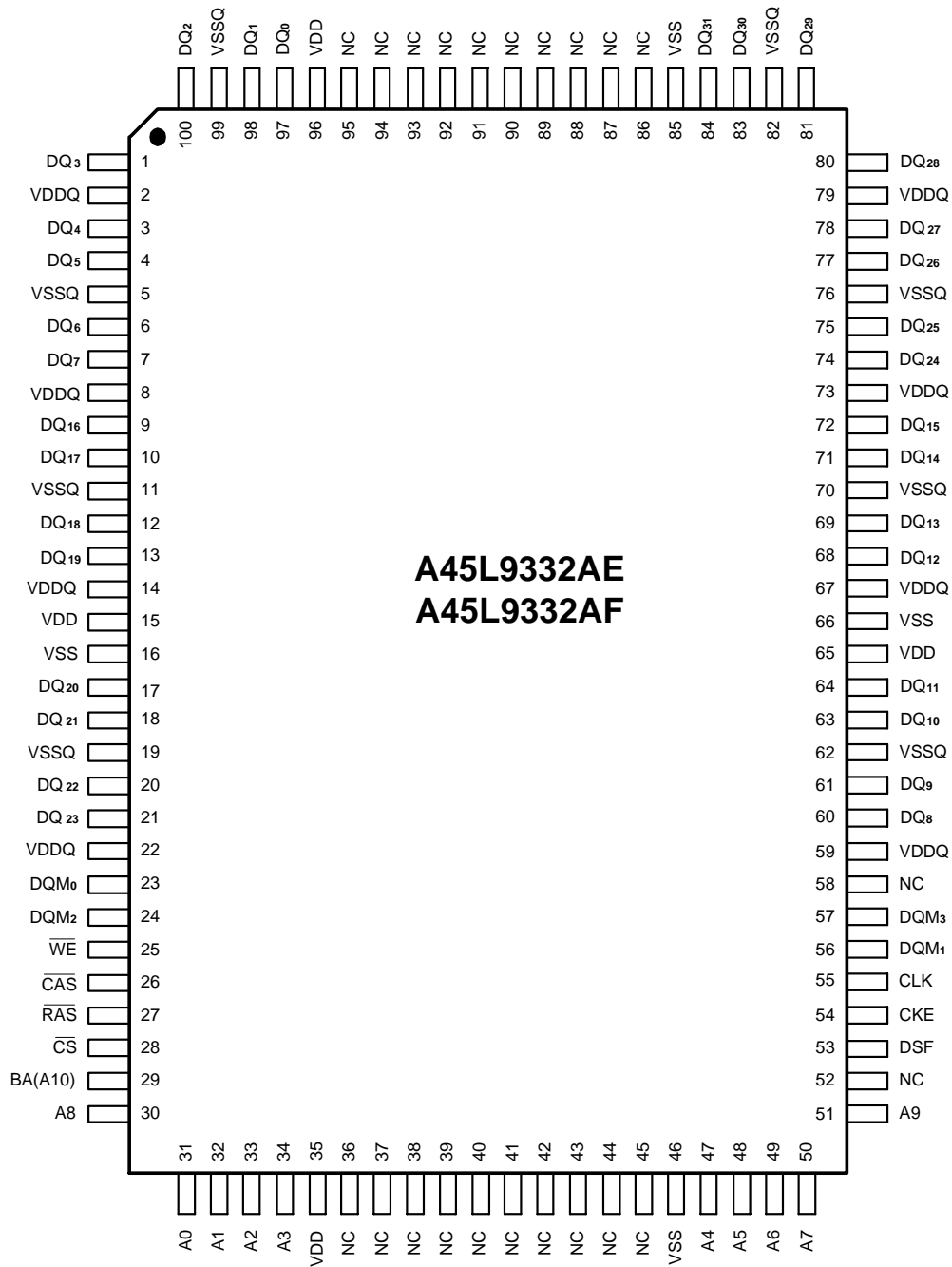### *Graphics Features*

- SMRS cycle
  - Load mask register
  - Load color register
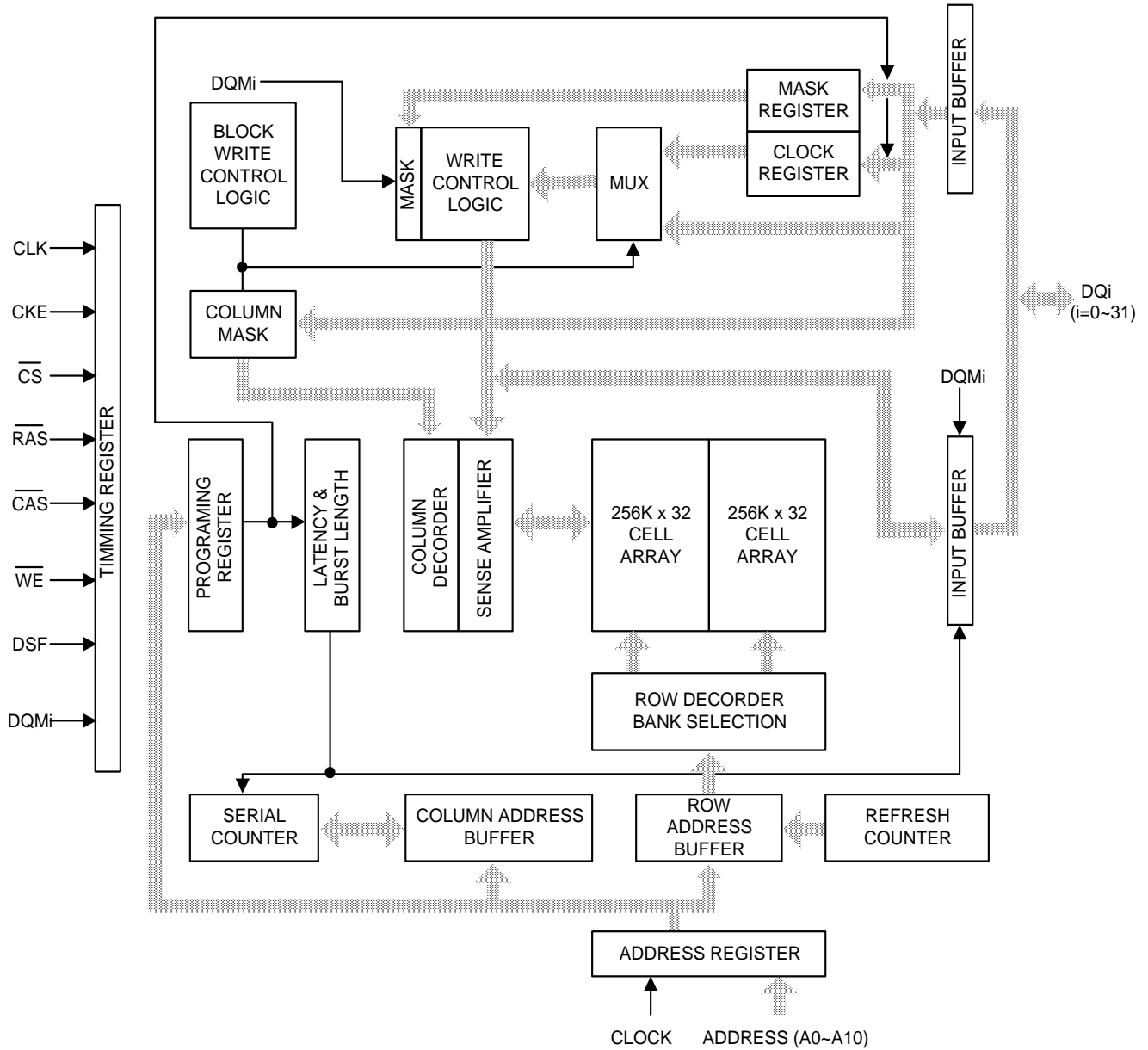- Write Per Bit (Old Mask)
- Block Write (8 Columns)

General Description

The A45L9332A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 X 262,144 words by 32 bits, fabricated with AMIC's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Write per bit and 8 columns block write improves performance in graphics system.

Pin Configuration

Top row pins (100 to 81): DQ2, VSSQ, DQ1, DQ0, VDD, NC, NC, NC, NC, NC, NC, NC, NC, NC, NC, VSS, DQ31, DQ30, VSSQ, DQ29

Left column pins (1 to 30):
Pin	Signal
1	DQ3
2	VDDQ
3	DQ4
4	DQ5
5	VSSQ
6	DQ6
7	DQ7
8	VDDQ
9	DQ16
10	DQ17
11	VSSQ
12	DQ18
13	DQ19
14	VDDQ
15	VDD
16	VSS
17	DQ20
18	DQ21
19	VSSQ
20	DQ22
21	DQ23
22	VDDQ
23	DQM0
24	DQM2
25	$\overline{WE}$
26	$\overline{CAS}$
27	$\overline{RAS}$
28	$\overline{CS}$
29	BA(A10)
30	A8

Center: **A45L9332AE A45L9332AF**

Right column pins (80 to 51):
Pin	Signal
80	DQ28
79	VDDQ
78	DQ27
77	DQ26
76	VSSQ
75	DQ25
74	DQ24
73	VDDQ
72	DQ15
71	DQ14
70	VSSQ
69	DQ13
68	DQ12
67	VDDQ
66	VSS
65	VDD
64	DQ11
63	DQ10
62	VSSQ
61	DQ9
60	DQ8
59	VDDQ
58	NC
57	DQM3
56	DQM1
55	CLK
54	CKE
53	DSF
52	NC
51	A9

Bottom row pins (31 to 50): A0, A1, A2, A3, VDD, NC, NC, NC, NC, NC, NC, NC, NC, NC, NC, VSS, A4, A5, A6, A7

Block Diagram

Pin Descriptions

Symbol	Name	Description
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or Enables device operation by masking or enabling all inputs except CLK, CKE and DQMi
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + t ss prior to new command. Disable input buffers for power down in standby.
A0~A9	Address	Row / Column addresses are multiplexed on the same pins. Row address : RA0~RA9, Column address: CA0~CA7
A10(BA)	Bank Select Address	Selects bank to be activated during row address latch time. Selects band for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
DQMi	Data Input/Output Mask	Makes data output Hi-Z, t SHZ after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DQi	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
DSF	Define Special Function	Enables write per bit, block write and special mode register set.
VDD/VSS	Power Supply/Ground	Power Supply: +3.3V$\pm$0.3V/Ground
VDDQ/VSSQ	Data Output Power/Ground	Provide isolated Power/Ground to DQs for improved noise immunity.
NC	No Connection	

Absolute Maximum Ratings*

Voltage on any pin relative to VSS (Vin, Vout) . . . . -1.0V to +4.6V
Voltage on VDD supply relative to VSS (VDD, VDDQ) . . . . -1.0V to +4.6V
Storage Temperature (T$_{STG}$) . . . . -55°C to +150°C
Soldering Temperature X Time (T$_{SLODER}$) . . . . 260°C X 10sec
Power Dissipation (P$_D$) 1W
Short Circuit Current (Ios) 50mA

*Comments

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Capacitance (T$_A$=25°C, f=1MHz)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	CI1	A0 to A9, BA	2		4	pF
	CI2	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMi, DSF	2		4	pF
Data Input/Output Capacitance	CI/O	DQ0 to DQ15	2		6	pF

DC Electrical Characteristics

Recommend operating conditions (Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD,VDDQ	3.0	3.3	3.6	V	
Input High Voltage	V$_{IH}$	2.0	3.0	VDD+0.3	V	
Input Low Voltage	V$_{IL}$	-0.3	0	0.8	V	Note 1
Output High Voltage	V$_{OH}$	2.4	-	-	V	Ioh = -2mA
Output Low Voltage	V$_{OL}$	-	-	0.4	V	Iol = 2mA
Input Leakage Current	I$_{IL}$	-5	-	5	µA	Note 2
Output Leakage Current	I$_{OL}$	-5	-	5	µA	Note 3
Output Loading Condition		See Figure 1				

Note: 1. V$_{IL}$ (min) = -1.5V AC (pulse width ≤ 5ns).
2. Any input 0V ≤ VIN ≤ VDD + 0.3V, all other pins are not under test = 0V
3. Dout is disabled, 0V ≤ Vout ≤ VDD

Decoupling Capacitance Guide Line

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between VDD and VSS	C$_{DC1}$	0.1 + 0.01	µF
Decoupling Capacitance between VDDQ and VSSQ	C$_{DC2}$	0.1 + 0.01	µF

Note: 1. VDD and VDDQ pins are separated each other.
All VDD pins are connected in chip. All VDDQ pins are connected in chip.
2. VSS and VSSQ pins are separated each other
All VSS pins are connected in chip. All VSSQ pins are connected in chip.

DC Electrical Characteristics

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

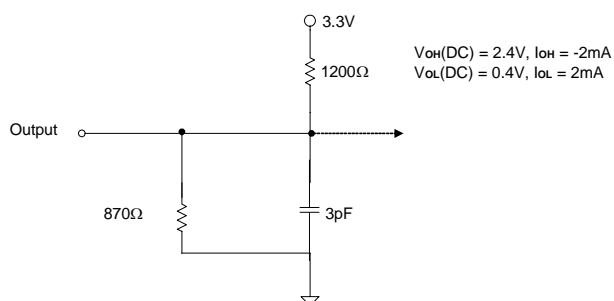| Symbol	Parameter	Test Conditions		CAS Latency	Speed			Unit	Notes
					-6	-7	-8		
I_{cc1}	Operating Current (One Bank Active)	Burst Length = 1		3	230	210	170	mA	1
		$t_{RC} \geq t_{RC}$(min), tcc $\geq$ tcc(min), I_{OL} = 0mA		2	-	260	160		
I_{cc2} P	Precharge Standby Current in power-down mode	CKE $\leq V_{IL}$(max), tcc = 15ns		4				mA	
I_{cc2} PS		CKE $\leq V_{IL}$(max), CKL $\leq$ VIL(max), tcc = ∞		4					
I_{cc2}N	Precharge Standby Current in non power-down mode	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		35				mA	
I_{cc2}NS		CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable.		15					
I_{cc3} P	Active Standby Current in power-down mode	CKE $\leq V_{IL}$(max), tcc = 15ns		6				mA	
I_{cc3} PS		CKE $\leq V_{IL}$(max), CKE $\leq V_{IL}$(max) tcc = ∞		6					
I_{cc3}N	Active Standby current in non power-down mode (One Bank Active)	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		60				mA	
I_{cc3}NS		CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable.		40					
I_{cc4}	Operating Current (Burst Mode)	I_{OL} = 0mA, Page Burst		3	310	280	250	mA	1
		All bank Activated, tccD = tccD (min)		2	-	230	210		
I_{cc5}	Refresh Current	$t_{RC} \geq t_{RC}$ (min)		3	150	120	120	mA	2
				2	-	180	120		
I_{cc6}	Self Refresh Current	CKE $\leq$ 0.2V		4				mA	
I_{cc7}	Operating Current (One Bank Block Write)	tcc $\geq$ tcc (min), I_{OL}=0mA, tBWC(min)		240	220	190		mA	

Note: 1. Measured with outputs open. Addresses are changed only one time during tcc(min).

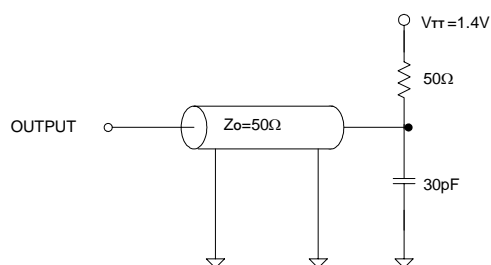2. Refresh period is 32ms. Addresses are changed only one time during tcc(min).

AC Operating Test Conditions

(VDD = 3.3V $\pm$0.3V, T$_A$ = 0°C to +70°C)

Parameter	Value
AC input levels	V$_{IH}$/V$_{IL}$ = 2.4V/0.4V
Input timing measurement reference level	1.4V
Input rise and all time (See note3)	tr/tf = 1ns/1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig.2

V$_{OH}$(DC) = 2.4V, I$_{OH}$ = -2mA
V$_{OL}$(DC) = 0.4V, I$_{OL}$ = 2mA

(Fig. 1) DC Output Load Circuit

(Fig. 2) AC Output Load Circuit

AC Characteristics

(AC operating conditions unless otherwise noted)

Symbol	Parameter	CAS Latency	-6		-7		-8		Unit	Note
			Min	Max	Min	Max	Min	Max		
tcc	CLK cycle time	3	6	1000	7	1000	8	1000	ns	1
		2	-		8		10			
tSAC	CLK to valid Output delay	3	-	5.5	-	6	-	6.5	ns	1,2
		2	-	-	-	7.5	-	7		
tOH	Output data hold time		2.5		2.5		2.5		ns	2
tCH	CLK high pulse width	3	2.5	-	2.5	-	3	-	ns	3
		2	-		3		3			
tCL	CLK low pulse width	3	2.5	-	2.5	-	3	-	ns	3
		2	-		3					
tSS	Input setup time	3	2	-	2	-	2.5	-	ns	3
		2	-		2.5					
tSH	Input hold time	3	1	-	1	-	1	-	ns	3
		2								
tSLZ	CLK to output in Low-Z	3	1	-	1	-	1	-	ns	2
		2								
tSHZ	CLK to output In Hi-Z	3	-	5.5	-	6	-	6.5	ns	
		2	-	-	-	7.5	-	7		

*All AC parameters are measured from half to half.

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Operating AC Parameter

(AC operating conditions unless otherwise noted)

Symbol	Parameter	CAS Latency	Version			Unit	Note
			-6	-7	-8		
$t_{RRD(min)}$	Row active to row active delay	3	2	2	2	CLK	1
		2					
$t_{RCD(min)}$	$\overline{RAS}$ to $\overline{CAS}$ delay	3	3	3	2	CLK	1
		2	-	2	2		
$t_{RP(min)}$	Row precharge time	3	3	3	2	CLK	1
		2	-	3	2		
$t_{RAS(min)}$	Row active time	3	8	7	6	CLK	1
		2	-	5	5		
$t_{RAS(max)}$		3	100			µS	
		2					
$t_{RC(min)}$	Row cycle time	3	11	10	9	CLK	1
		2	-	7	7		
$t_{CDL(min)}$	Last data in new col. Address delay	3	1			CLK	2
		2					
$t_{RDL(min)}$	Last data in row precharge	3	2	2	2	CLK	2
		2	-	2	2		
$t_{BDL(min)}$	Last data in to burst stop	3	1			CLK	2
		2					
$t_{CCD(min)}$	Col. Address to col. Address delay	3	1			CLK	3
		2					
$t_{BPL(min)}$	Block write data-in to PRE command	3	2			CLK	
		2					
$t_{BWC(min)}$	Block write cycle time	3	1			CLK	1,3
		2					
Number of valid output data		3	2			CLK	4
		2	1			CLK	

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. This parameter means minimum $\overline{CAS}$ to $\overline{CAS}$ delay at block write cycle only.
4. In case of row precharge interrupt, auto precharge and read burst stop.

Simplified Truth Table

Command			CKEn-1	CKEn	C̄S̄	R̄ĀS̄	C̄ĀS̄	W̄Ē	DSF	DQM	A10	A9	A8~A0	Notes
Register	Mode Register Set		H	X	L	L	L	L	L	X	OP CODE			1,2
	Special Mode Register Set								H					1,2,7
Refresh	Auto Refresh		H	H	L	L	L	H	L	X	X			3
	Self	Entry		L										3
	Refresh	Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active	Write Per Bite Disable		H	X	L	L	H	H	L	X	V	Row Addr.		4,5
& Row Addr.	Write Per Bit Enable								H					4,5,9
Read &	Auto Precharge Disable		H	X	L	H	L	H	L	X	V	L	Column	4
Column Addr.	Auto Precharge Enable											H	Addr.	4,6
Write &	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column	4,5
Column Addr.	Auto Precharge Enable											H	Addr.	4,5,6,9
Block Write &	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column	4,5
Column Addr.	Auto Precharge Enable											H	Addr.	4,5,6,9
Burst Stop			H	X	L	H	H	L	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	L	X	V	L	X	
	Both Banks										X	H		
Clock Suspend or		Entry	H	L	L	H	H	H	X	X	X			
Active Power Down					H	X	X	X						
		Exit	L	H	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	L	V	V	V	V	X				
					H	X	X	X	X					
DQM			H		X					V	X			8
No Operation Command			H	X	L	H	H	H	X	X	X			
					H	X	X	X						

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Note : 1. OP Code : Operand Code
   A0~A10 : Program keys. (@MRS)
   Color register exists only one per DQi which both banks share.
   So dose Mask Register.
   Color or mask is loaded into chip through DQ pin.
   2. MRS can be issued only at both banks precharge state.
   SMRS can be issued only if DQ's are idle.
   A new command can be issued at the next clock of MRS/SMRS.
   3. Auto refresh functions as same as CBR refresh of DRAM.
   The automatical precharge without Row precharge command is meant by "Auto".
   Auto/Self refresh can be issued only at both precharge state.
   4. A10 : Bank select address.
   If "Low" at read, (block) write, Row active and precharge, bank A is selected.
   If "High" at read, (block) write, Row active and precharge, bank B is selected.
   If A9 is "High" at Row precharge, A10 is ignored and both banks are selected.
   5. It is determined at Row active cycle.
   whether Normal/Block write operates in write per bit mode or not.
   For A bank write, at A bank Row active, for B bank write, at B bank Row active.
   Terminology : Write per bit = I/O mask
           (Block) Write with write per bit mode = Masked (Block) Write

Simplified Truth Table

    6. During burst read or write with auto precharge, new read/ (block) write command cannot be issued.
       Another bank read/(block) write command can be issued at tᴘʀ after the end of burst.
    7. Burst stop command is valid only t full page burst length.
    8. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
       but makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2)
    9. Graphic features added to SDRAM's original features.
       If DSF is tied to low, graphic functions are disabled and chip operates as a 16M SDRAM with 32 DQ's.

SGRAM vs SDRAM

Function	MRS		Bank Active		Write	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

<u>IF DSF is low, SGRAM functionality is identical to SDRAM functionality.</u>

SGRAM can be used as an unified memory by the appropriate DSF control
→SDRAM = Graphic Memory + main Memory

Mode Register Filed Table to Program Modes

Register Programmed with MRS

Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

     (Note 1)   (Note 2)

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor	0	0	1	-	1	Interleave	0	0	1	2	Reserved
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)	Reserved

                                                                            (Note 3)

Special Mode Register Programmed with SMRS

Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	X				LC	LM	X				

Load Color		Load Mask	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

(Note 4)

Power Up Sequence

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. RFU(Reserved for Future Use) should stay "0" during MRS cycle.
   2. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
   3. The full column burst (256bit) is available only at Sequential mode of burst type.
   4. If LC and LM both high (1), data of mask and color register will be unknown.

Burst Sequence (Burst Length = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst Sequence (Burst Length = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Pixel to DQ Mapping (at BLOCK WRITE)

Column address			3 Byte	2 Byte	1 Byte	0 Byte
A2	A1	A0	$I/O_{31} - I/O_{24}$	$I/O_{23} - I/O_{16}$	$I/O_{15} - I/O_8$	$I/O_7 - I/O_0$
0	0	0	DQ24	DQ16	DQ8	DQ0
0	0	1	DQ25	DQ17	DQ9	DQ1
0	1	0	DQ26	DQ18	DQ10	DQ2
0	1	1	DQ27	DQ19	DQ11	DQ3
1	0	0	DQ28	DQ20	DQ12	DQ4
1	0	1	DQ29	DQ21	DQ13	DQ5
1	1	0	DQ30	DQ22	DQ14	DQ6
1	1	1	DQ31	DQ23	DQ15	DQ7

Device Operations

Clock (CLK)

The clock input is used as the reference for all SGRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between VIL and VIH. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set up and hold time around positive edge of the clock for proper functionality and ICC specifications.

Clock Enable (CLK)

The clock enable (CKE) gates the clock onto SGRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended form the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SGRAM enters the power down mode form the next clock cycle. The SGRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "tSS + 1 CLOCK" before the high going edge of the clock, then the SGRAM becomes active from the same clock edge accepting all the input commands.

Bank Select (A10)

This SGRAM is organized as two independent banks of 262,144 words X 32 bits memory arrays. The A10 input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A10 is asserted low, bank A is selected. When A10 is asserted high, bank B is selected. The bank select A10 is latched at bank activate, read, write mode register set and precharge operations.

Address Input (A0 ~ A9)

The 18 address bits required to decode the 262,144 word locations are multiplexed into 10 address input pins (A0~A9). The 10 bit row address is latched along with $\overline{RAS}$ and A10 during bank activate command. The 8 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A10 during read or write command.

NOP and Device Deselect

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SGRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$, DSF and all the address inputs are ignored.

Power-Up

The following sequence is recommended for POWER UP
1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the inputs before or along with VDD (and VDDQ) supply. The clock signal must also be asserted at the same time.
2. After VDD reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined.
   At the end of one clock cycle from the mode register set cycle, the device is ready for operation.
   When the above sequence is used for Power-up, all the outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
   Cf.) Sequence of 4 & 5 may be charged.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of SGRAM. It programs the CAS latency, addressing mode, burst length, test mode and various vendor specific options to make SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SGRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF (The SGRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A9 and A10 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF going low is the data written in the mode register. One clock cycle is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A0~A2, burst type uses A3, addressing mode uses A4~A6, A7~A8 and A10 are used for vendor specific options or test mode. And the write burst length is programmed using A9. A7~A8 and A10 must be set to low for normal SGRAM operation.

Refer to table for specific codes for various burst length, addressing odes and CAS latencies.

Device Operations (continued)

Bank Activate

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of t$_{RCD}$(min) from the time of bank activation. t$_{RCD}$(min) is an internal timing parameter of SGRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t$_{RCD}$(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SGRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SGRAM is high requiring some time for power supplies recover before the other bank can be sensed reliably. t$_{RRD}$(min) specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to t$_{RCD}$ specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t$_{RAS}$(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t$_{RAS}$(max). The number of cycles for both t$_{RAS}$(min) and t$_{RAS}$(max) can be calculated similar to t$_{RCD}$ specification.

Burst Read

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t$_{RCD}$(min) before the burst read command is issued. The first output appears CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid only at full page burst length where the output dose not go into high impedance at the end of burst and the burst is wrap around.

Burst Write

The burst write command is similar to burst read command, and is used to write data into the SGRAM consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can not complete to burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid only at full page burst length where the writing continues at the end of burst and the burst is wrap around. The write burst can also be terminated by using DQM for blocking data and precharging the bank "t$_{RDL}$" after the last data input to be written into the active row. See DQM OPERATION also.

DQM Operation

The DQM is used to mask input and output operation. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SGRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. DQM is also used for device selection, byte selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. DQM masks the DQ's by a byte regardless that the corresponding DQ's are in a state of WPB masking or Pixel masking. Please refer to DQM timing diagram also.

Precharge

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A9 with valid A10 of the bank to be precharged. The precharge command can be asserted anytime after t$_{RAS}$(min) is satisfied from the bank activate command in the desired bank. "t$_{RP}$" is defined as the minimum time required to precharge a bank.
The minimum number of clock cycles required to complete row precharge is calculated by dividing "t$_{RP}$" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t$_{RAS}$(max). Therefore, each bank has to be precharged within t$_{RAS}$(max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again.
Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc, is possible only when both banks are in idle state.

Device Operations (continued)

Auto Precharge

The precharge operation can also be performed by using auto precharge. The SGRAM internally generates the timing to satisfy t$_{RAS}$(min) and "t$_{RP}$" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A9. If burst read or burst write command is issued with low on A9, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

Both Banks Precharge

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ with high on A9 after both banks have satisfied t$_{RAS}$(min) requirement, performs precharge on both banks. At the end of tRP after performing precharge all, both banks are in idle state.

Auto Refresh

The storage cells of SGRAM need to be refreshed every 32ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by "t$_{RC}$(min)". The minimum number of clock cycles required can be calculated by driving "t$_{RC}$" with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SGRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 2048 auto refresh cycles once in 32ms.

Self Refresh

The self refresh is another refresh mode available in the SGRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SGRAM. In self refresh mode, the SGRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of "t$_{RC}$" before the SGRAM reaches idle

state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to used burst 2048 auto refresh cycles immediately after exiting self refresh.

Define Special Function (DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM function is 256K X 32 X 2 Bank SDRAM. SDRAM can be used as an unified memory by the appropriate DSF command. All the graphic function mode can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands.
SDRAM functions such as $\overline{RAS}$ Active, Write, and WCBR change to SGRAM functions such as $\overline{RAS}$ Active with WPB, Block Write and SWCBR respectively. See the sessions below for the graphic functions that DSF controls.

Special Mode Register Set (SMRS)

There are two kinds of special mode registers in SGRAM. One is color register and the other is mask register. Those usage will be explained at "WRITE PER BIT" and "BLOCK WRITE" session. When A5 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, load mask register (LMR) process is executed and the mask registers are filled with the masks for associated DQ's through DQ pins. And when A6 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, load color register (LCR) process is executed and the color register is filled with color data for associated DQ's through the DQ pins. If both A5 and A6 are high at SMRS, data of mask and color cycle is required to complete the write in the mask register and the color register at LMR and LCR respectively. The next clock of LMR or LCR, a new commands can be issued. SMRS, compared with MRS, can be issued at the active state under the condition that DQ's are idle. As in write operation, SMRS accepts the data needed through DQ pins. Therefore it should be attended not to induce bus contention. The more detailed materials can obtained by referring corresponding timing diagram.

Write Per Bit

Write per bit (i.e. I/O mask mode) for SGRAM is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enabled. Bank active command with DSF = High enabled write per bit operations is stored in the mask register accessed by SWCBR (Special Mode Register Set Command). When a mask bit = 1, the associated data bit is written when a write command is executed and write per bit has been enabled for the bank being written. When a mask bit = 0, the associated data bit is unaltered when a write command is executed and the write per bit has been enabled for the bank being written. No additional timing conditions are required for write per bit operations. Write per bit writes can be either single write, burst writes or block writes. DQM masking is the same for write per bit and non-WPB write.
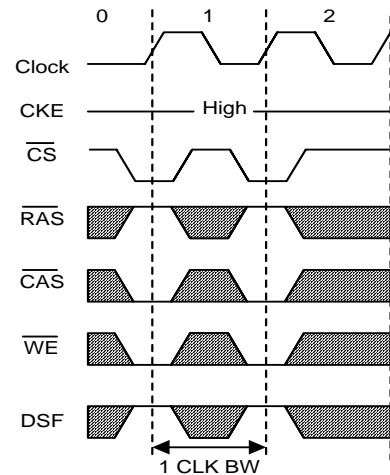
Device Operations (continued)

Block Write

Block write is a feature allowing the simultaneous writing of consecutive 8 columns of data within a RAM device during a single access cycle. During block write the data to be written comes from an internal "color" register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8 column boundaries and is defined by the column address with the 3 LSB's ignored. Write command with DSF = 1enables block write for the associated bank. A write command with DSF = 0 enables normal write for the associated bank. The block width is 8 column where column = "n" bits for by "n" part. The color register is the same width as the data port of the chip. It is written via a SWCBR where data present on the DQ pin is to be coupled into the internal color register. The color register provides the data masked by the DQ column select, WPB mask (If enabled), and DQM byte mask. Column data masking (Pixel masking) is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per bit basis (i.e. DQ[0:7] provides the column mask for data bits[0:7], DQ[8:15] provides the column mask for data bits[8:15], DQ0 masks column[0] for data bits[0:7], DQ9 masks column [1] for data its [8:15], etc). Block writes are always non-burst, independent of the burst length that has been programmed into the mode register. Back to back block writes are allowed provided that the specified block write cycle time (t_{BWC}) is satisfied. If write per bit was enabled by the bank active command with DSF = 1, then write per bit masking of the color register data is enabled.
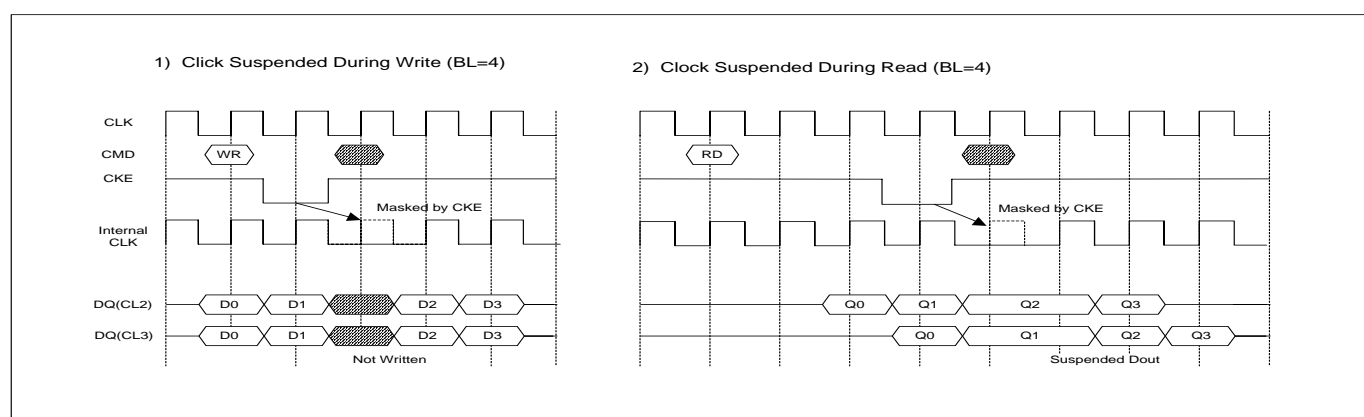
If write per bit was disabled by a bank active command with DSF = 0, the write per bit masking of the color register data is disabled. DQM masking provides independent data byte masking during block write exactly the same as it does during normal write operations, except that the control is extended to the consecutive 8 columns of the block write.

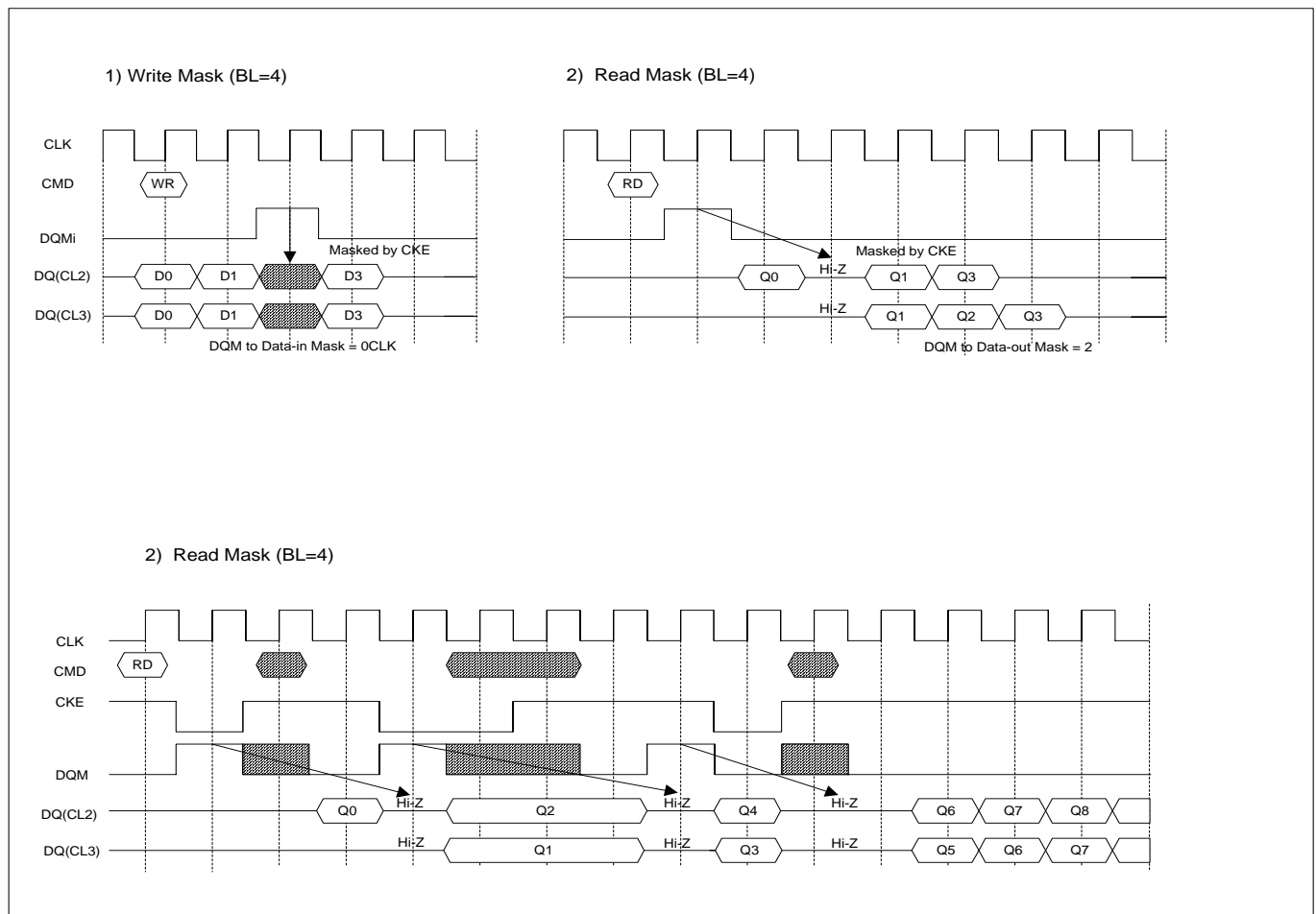### Timing Diagram to Illustrate t_{BWC}

AMIC   *A45L9332A Series*
Summary of 2M Byte SGRAM Basic Features and Benefits

Features	256K X 32 X 2 SGRAM	Benefits
Interface	Synchronous	Better interaction between memory and system without wait-state of asynchronous DRAM. High speed vertical and horizontal drawing. High operation frequency allows performance gain for SCROLL, FILL, and BitBLT.
Bank	2 ea	Pseudo-infinite row length by on-chip interleaving operation. Hidden row activation and precharge.
Page Depth / 1 Row	256 bit	High speed vertical and horizontal drawing.
Total Page Depth	2048 bytes	High speed vertical and horizontal drawing
Burst Length (Read)	1,2,4,8 Full Page	Programmable burst of 1,2,4,8 and full page transfer per column addresses.
Burst Length (Write)	1,2,4,8 Full Page	Programmable burst of 1,2,4,8 and full page transfer per column addresses.
	BRSW	Switch to burst length of 1 at write without MRS
Burst Type	Sequential & Interleave	Compatible with Intel and Motorola CPU based system.
CAS Latency	2,3	Programmable CAS latency.
Block Write	8 Columns	High speed FILL, CLEAR, Text with color registers. Maximum 32 byte data transfers (e.g. for 8bpp : 32 pixels) with plane and byte masking functions.
Color Register	1 ea.	A and B bank share.
Mask Register	1 ea.	Write-per-bit capability (bit plane masking). A and B banks share.
Mask function	DQM0-3	Byte masking (pixel masking for 8bpp system) for data-out/in
	Write per bit	Each bit of the mask register directly controls a corresponding bit plane.
	Pixel Mask at Block Write	Byte masking (pixel masking for 8bpp system) for color by DQi

Basic feature And Function Descriptions

1. CLOCK Suspend

Note: CLK to CLK disable/enable=1 clock

(August, 2004, Version 1.1)   18   **AMIC Technology, Corp.**

2. DQM Operation

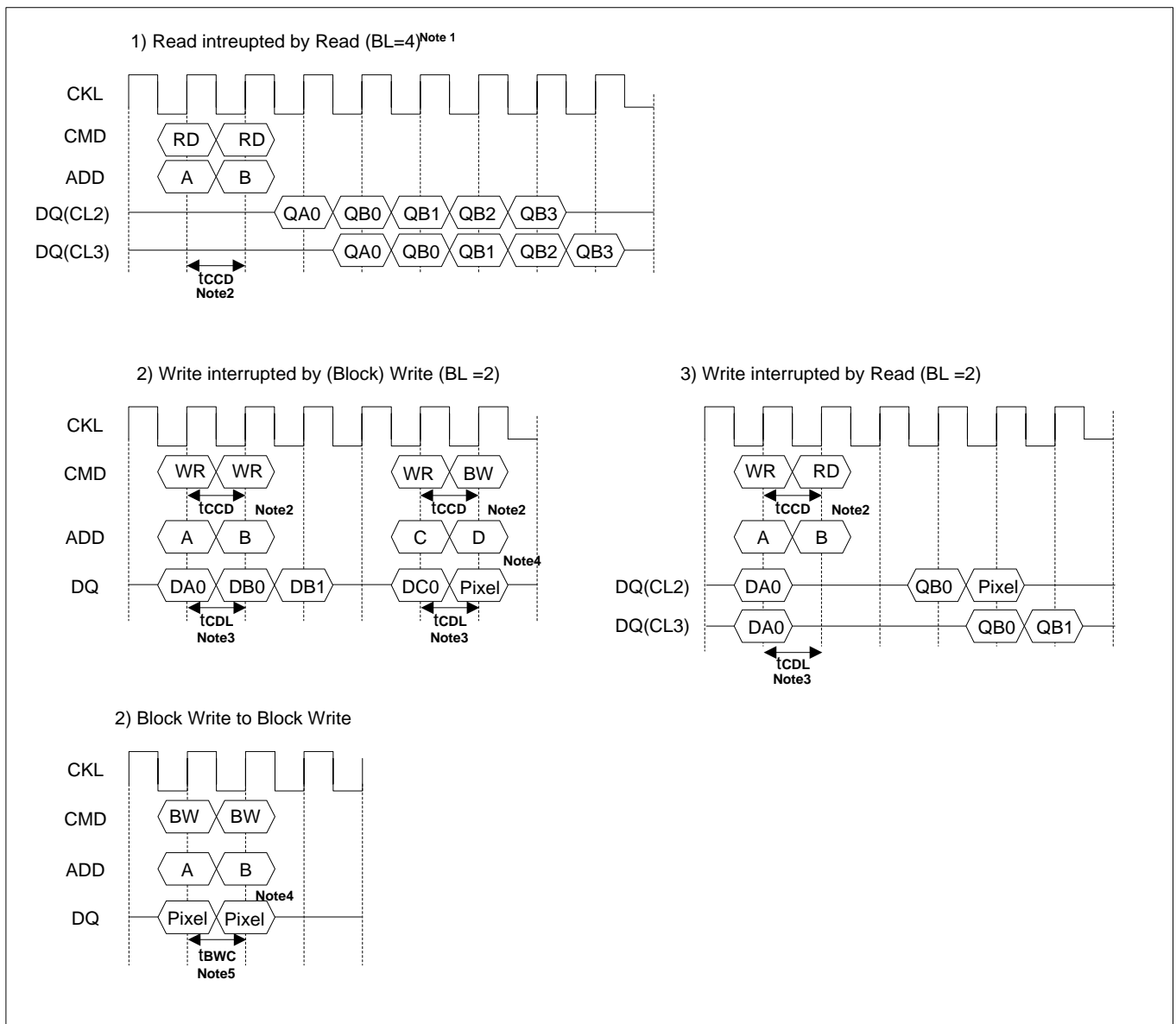1) Write Mask (BL=4)

2) Read Mask (BL=4)

2) Read Mask (BL=4)

* **Note :** 1. There are 4 DQMi (I=0~3).

Each DQMi masks 8 DQi's. (1 Byte, 1 Pixel for 8bbp).

2. DQM makes data out Hi-Z after 2 clocks which should masked by CKE "L".

3. CAS Interrupt (I)

1) Read intreupted by Read (BL=4)[Note 1]

2) Write interrupted by (Block) Write (BL =2)

3) Write interrupted by Read (BL =2)

2) Block Write to Block Write

Note : 1. By "Interrupt", It is possible to stop burst read/write by external command before the end of burst.

By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access; read, write and block write.

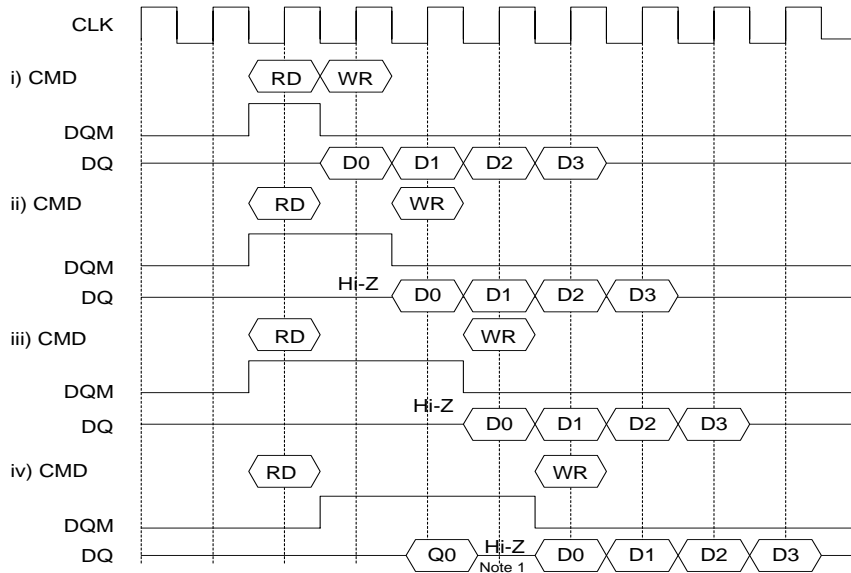2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)

3. tCDL : Last data in to new column address delay. (= 1CLK).

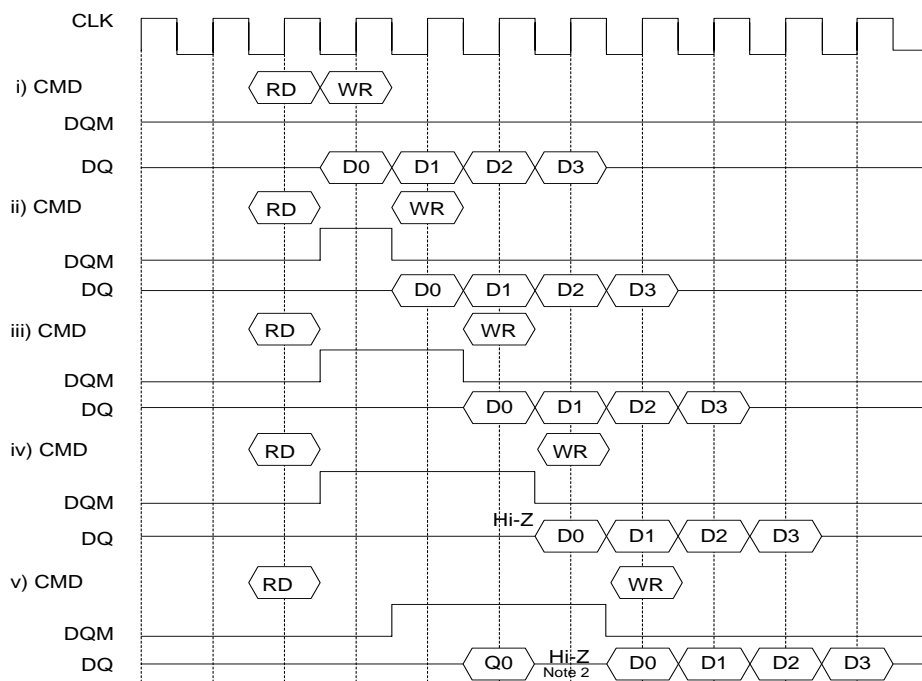4. Pixel : Pixel mask.

5. t_{BWC} : Block write minimum cycle time.

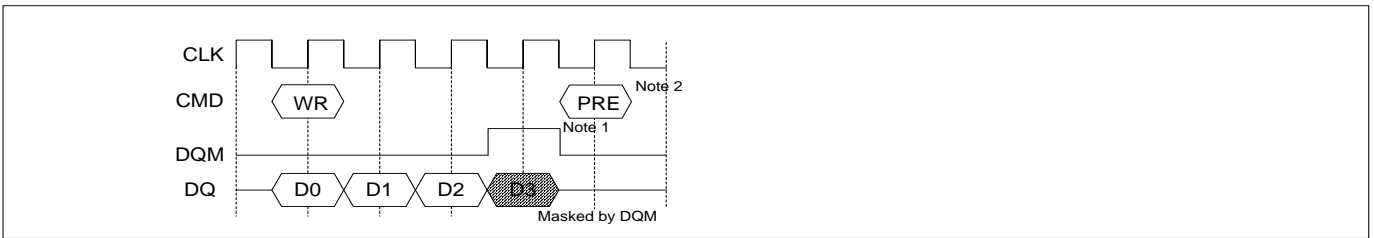## 4. CAS Interrupt (II) : Read Interrupted Write & DQM

(1) CL=2, BL=4

(2) CL=3, BL=4

* Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.
2. To prevent bus contention, DQM should be issued which makes a least one gap between data in and data out.
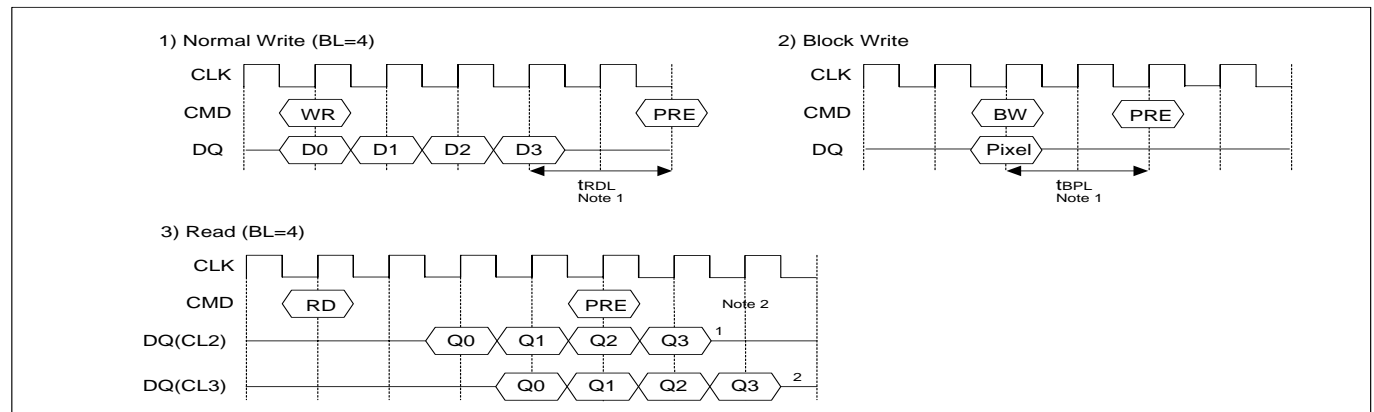
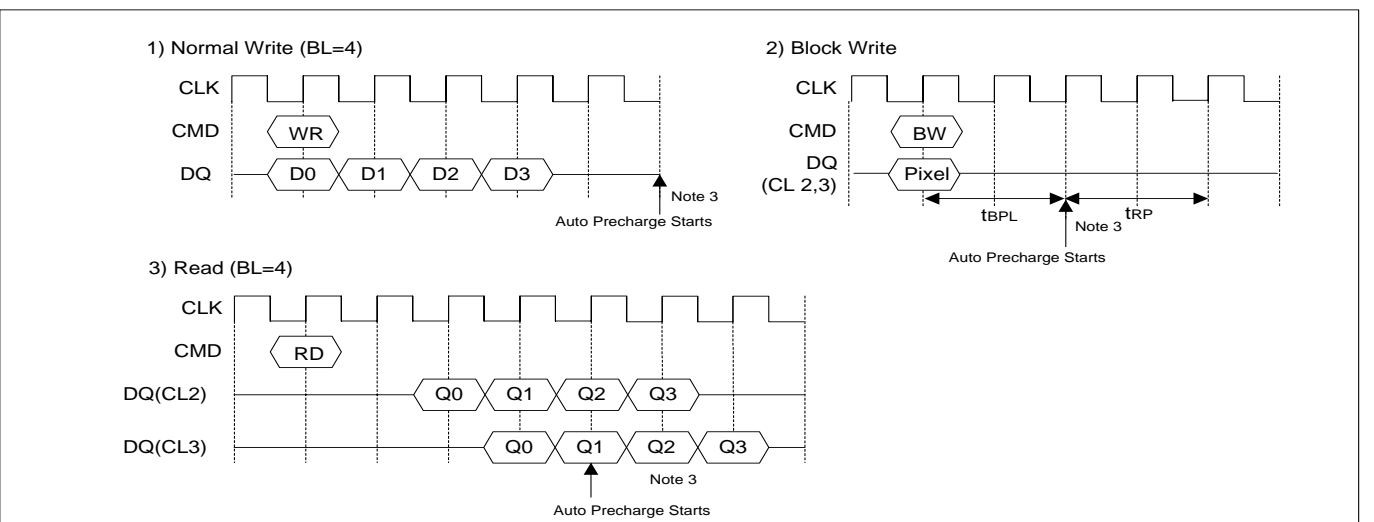### 5. Write Interrupted by Precharge & DQM

Note : 1. To inhibit invalid write, DQM should be issued.
    2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge
       interrupt but only another bank precharge of dual banks operation.

6. Precharge

7. Auto Precharge

* Note : 1. t_{BPL} : Block write data-in to PRE command delay.
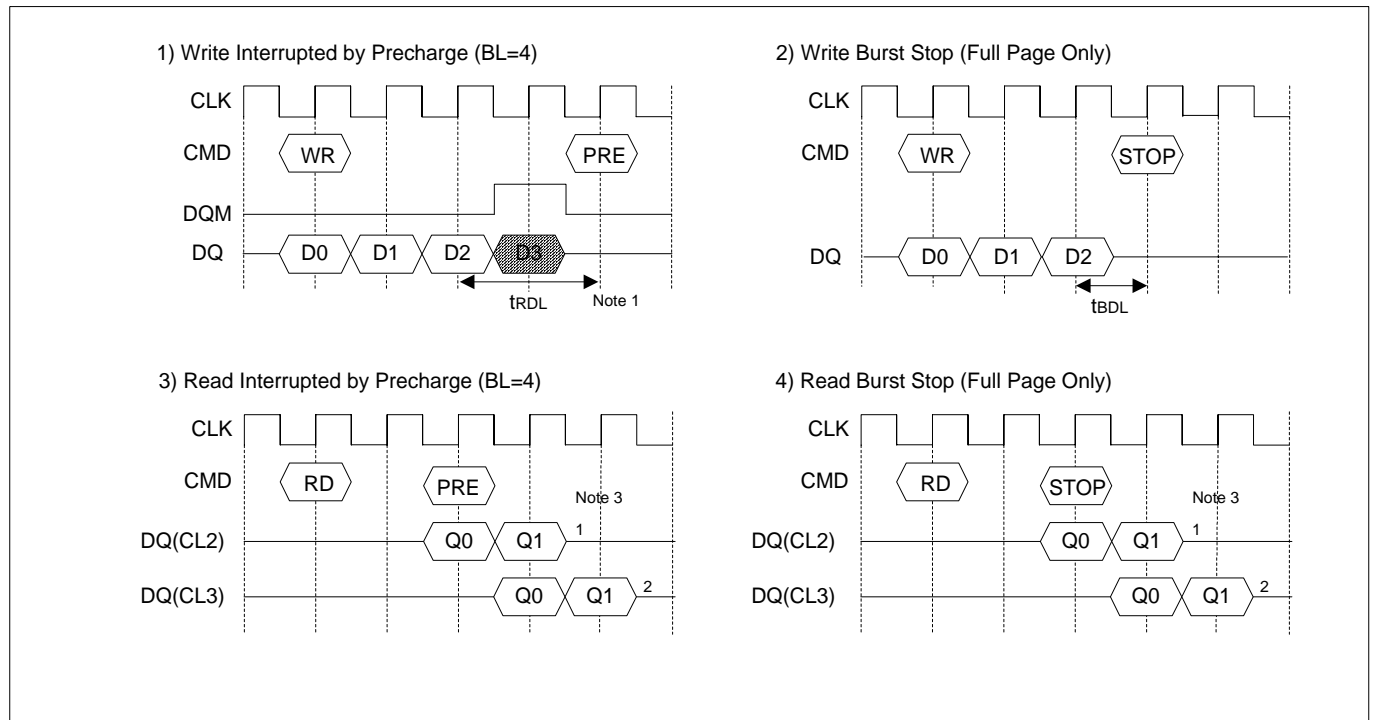   2. Number of valid output data after Row Precharge : 1,2 for CAS Latency = 2,3 respectively.
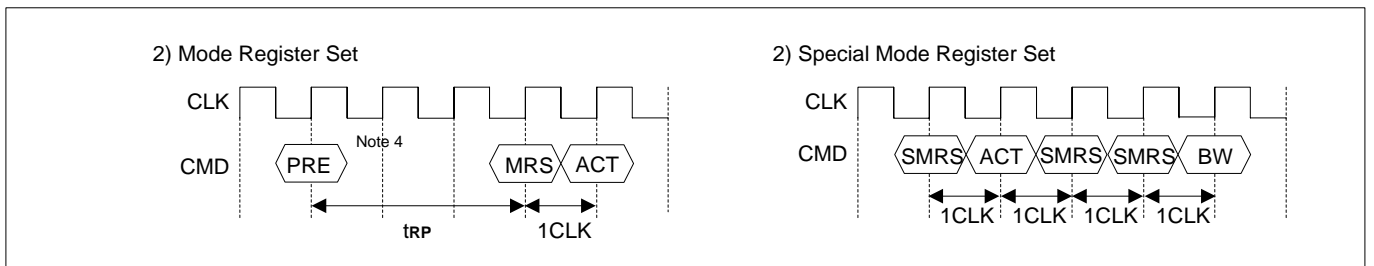   3. The row active command of the precharge bank can be issued after t_{RP} from this point.
       The new read/write command of other active bank can be issued from this point.
       At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

8. Burst Stop & Precharge Interrupt

1) Write Interrupted by Precharge (BL=4)

CLK

CMD ⟨ WR ⟩　　　　⟨ PRE ⟩

DQM

DQ ⟨ D0 ⟩⟨ D1 ⟩⟨ D2 ⟩⟨ D3 ⟩

t_{RDL}　Note 1

2) Write Burst Stop (Full Page Only)

CLK

CMD ⟨ WR ⟩　　　　⟨ STOP ⟩

DQ ⟨ D0 ⟩⟨ D1 ⟩⟨ D2 ⟩

t_{BDL}

3) Read Interrupted by Precharge (BL=4)

CLK

CMD ⟨ RD ⟩　　⟨ PRE ⟩　Note 3

DQ(CL2) ⟨ Q0 ⟩⟨ Q1 ⟩ 1

DQ(CL3) ⟨ Q0 ⟩⟨ Q1 ⟩ 2

4) Read Burst Stop (Full Page Only)

CLK

CMD ⟨ RD ⟩　⟨ STOP ⟩　Note 3

DQ(CL2) ⟨ Q0 ⟩⟨ Q1 ⟩ 1

DQ(CL3) ⟨ Q0 ⟩⟨ Q1 ⟩ 2

9. MRS & SMRS

2) Mode Register Set

CLK

CMD ⟨ PRE ⟩ Note 4　⟨ MRS ⟩⟨ ACT ⟩

t_{RP}　1CLK

2) Special Mode Register Set

CLK
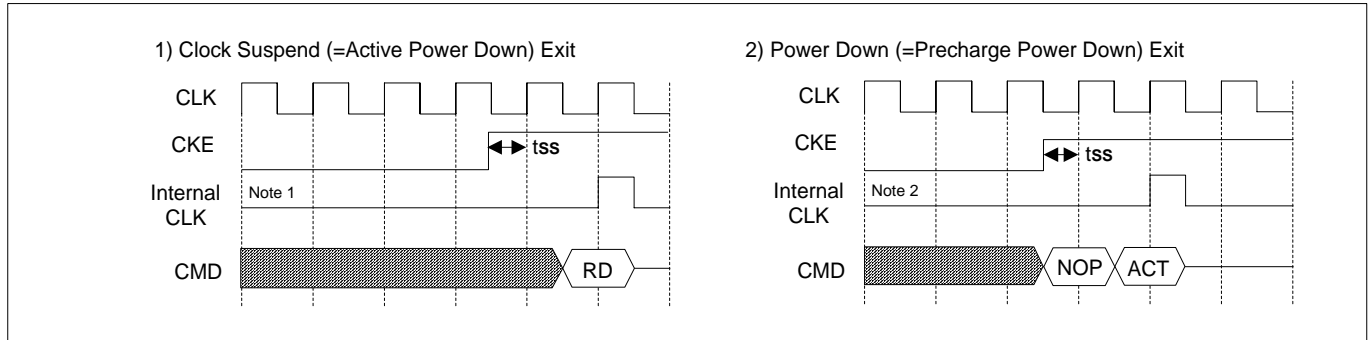
CMD ⟨ SMRS ⟩⟨ ACT ⟩⟨ SMRS ⟩⟨ SMRS ⟩⟨ BW ⟩
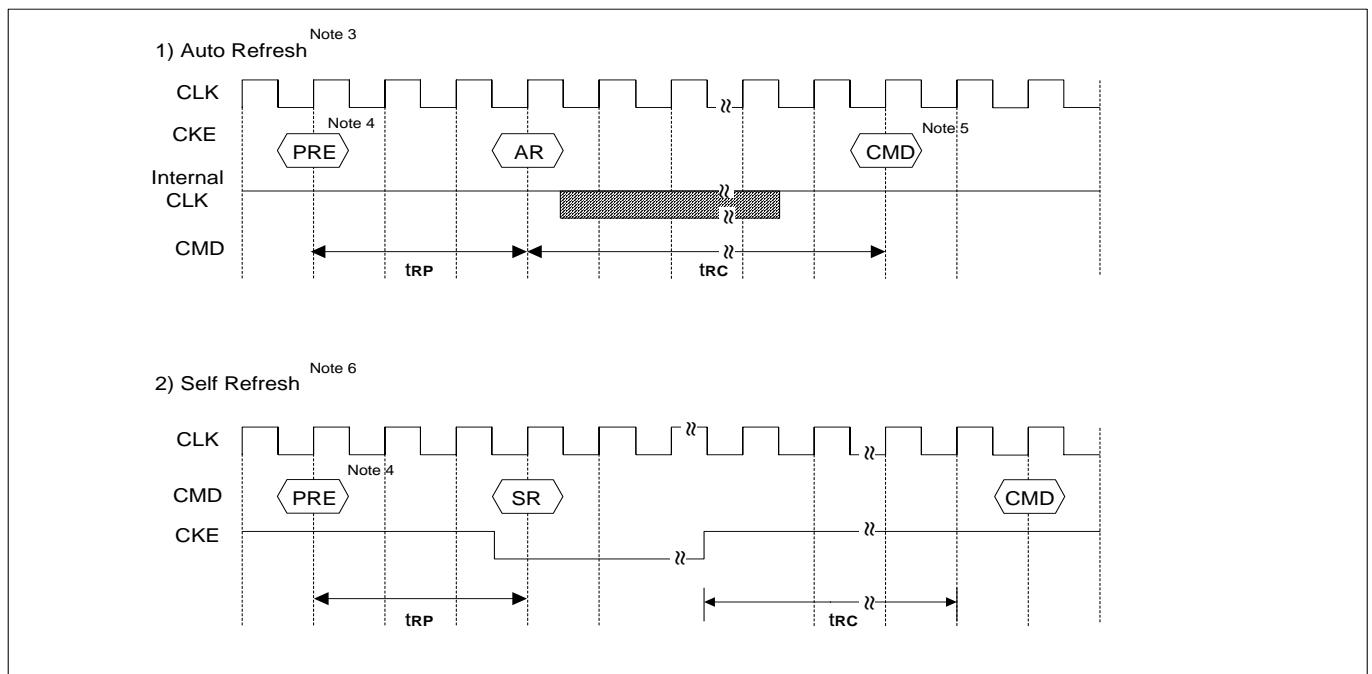
1CLK 1CLK 1CLK 1CLK

Note : 1. t_{RDL} : 2CLK, Last Data in to Row Precharge.
　　　2. t_{BDL} : 1CLK, Last Data in to Burst Stop Delay.
　　　3. Number of valid output data after Row precharge or burst stop : 1,2 for CAS latency=2,3 respectively.
　　　4. PRE : Both banks precharge if necessary.
　　　　MRS can be issued only at all bank precharge state.

10. Clock Suspend Exit & Power Down Exit

1) Clock Suspend (=Active Power Down) Exit

CLK

CKE
tss

Internal
CLK
Note 1

CMD
RD

2) Power Down (=Precharge Power Down) Exit

CLK

CKE
tss

Internal
CLK
Note 2

CMD
NOP   ACT

11. Auto Refresh & Self Refresh

1) Auto Refresh   Note 3

CLK

CKE   Note 4

PRE   AR   CMD   Note 5

Internal
CLK

CMD

t$_{RP}$ t$_{RC}$

2) Self Refresh   Note 6

CLK

CMD   Note 4

PRE   SR   CMD

CKE

t$_{RP}$ t$_{RC}$

* Note : 1. Active power down : one or more bank active state.
2. Precharge power down : both bank precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
   No precharge commands are required after Auto Refresh command.
   During t$_{RC}$ from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. (S)MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally.
   After self refresh entry, self refresh mode is kept while CKE is LOW.
   During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
   During t$_{RC}$ from self refresh exit command, any other command can not be accepted.
   Before/After self refresh mode, burst auto refresh cycle (2K cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential counting	At MRS A3="0". See the BURST SEQUENCE TABE.(BL=4,8) BL=1,2,4,8 and full page wrap around.
	Interleave counting	At MRS A3=" 1". See the BURST SEQUENCE TABE.(BL=4,8) BL=4,8 At BL=1,2 Interleave Counting = Sequential Counting
Pseudo-MODE	Pseudo-Decrement Sequential Counting	At MRS A3 = "1". (See to Interleave Counting Mode) Starting Address LSB 3 bits A0-2 should be "000" or "111".@BL=8. --if LSB = "000" : Increment Counting. --if LSB= "111" : Decrement Counting. For Example, (Assume Addresses except LSB 3 bits are all 0, BL=8) --@ write, LSB="000", Accessed Column in order 0-1-2-3-4-5-6-7 --@ read, LSB="111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at Interleave Counting mode, by confining starting address to some values, Pseudo-Decrement Counting Mode can be realized. See the BURST SEQUENCE TABLE carefully.
	Pseudo-Binary Counting	At MRS A3 = "0". (See to Sequential Counting Mode) 　　　　 A0-2 = "111". (See to Full Page Mode) Using Full Page Mode and Burst Stop Command, Binary Counting Mode can be realized. --@ Sequential Counting Accessed Column in order 3-4-5-6-7-1-2-3 (BL=8) --@ Pseudo-Binary Counting, Accessed Column in order 3-4-5-6-7-8-9-10 (Burst Stop command) Note. The next column address of 256 is 0
Random MODE	Random column Access tccD = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of convention DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS A2,1,0 = "000". At auto precharge, tRAS should not be violated.
	2	At MRS A2,1,0 = "001". At auto precharge, tRAS should not be violated.
	4	At MRS A2,1,0 = "010"
	8	At MRS A2,1,0 = "011".
	Full Page	At MRS A2,1,0 = "111". Wrap around mode (Infinite burst length) should be stopped by burst stop, $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt.
Special MODE	BRSW	At MRS A9="1". Read burst = 1,2,4,8, full page/write Burst =1 At auto precharge of write, tRAS should not be violated.
	Block Write	8 Column Block Write. LSB A0-2 are ignored. Burst length=1. tBWC should not be violated. At auto precharge, tRAS should not be violated.
Random MODE	Burst Stop	tBDL=1, Valid DQ after burst stop is 1,2 for CL=2,3 respectively Using burst stop command, it is possible only at full page burst length.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank Stops read/write burst with Row precharge. tRDL=2 with DQM, valid DQ after burst stop is 1,2 for CL=2,3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt cannot be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

14. Mask Functions

1) Normal Write

I/O masking : By Mask at Write per Bit Mode, the selected bit planes keep the original data.

If bit plane 0,3,7,9,15,22,24, and 31 keep the original value.

i) STEP

•• SMRS (LMR) : Load mask [31-0]="0111,1110,1011,1111,0111,1101,0111,0110"

•• Row Active with DSF "H" : Writ Per Bit Mode Enable

•• Perform Normal Write

ii) ILLUSTRATION

I/O(=DQ)	31 24	23 16	15 8	7 0
External Data-in	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	0 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1	0 1 1 1 1 0 1	0 1 1 0 0 1 1 0
Before Write	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
After Write	0 1 1 1 1 1 1 0	1 0 1 1 1 1 1 1	1 0 0 0 0 1 0	1 1 1 1 1 1 1 1

Note 1

2) Block Write

Pixel masking : By Pixel Data issued through DQ pin, the selected pixels keep the original data.

See PIXEL TO DQ MAPPING TABLE.

If Pixel 0,4,9,13,18, 22, 27 and 31 keep the original white color.

Assume 8bpp,

White = "0000,0000", Red = "1010,0011", Green = "1110,0001", Yellow = "0000,1111", Blue = "1100,0011"

i) STEP

•• SMRS(LCR) : Load color (for 8bbp, through X32 DQ color 0-3 are loaded into color registers)

Load(color3, color2, color1, color0) = (Blue, Green, Yellow, Red)

= "1100,0011,1110,0001,0000,1111,1010,0011"

•• Row Active with DSF "L" : I/O Mask by Write Per Bit Mode Disable

•• Block write with DQ[31-0] = "0111,0111,1011,1011,1101,1101,1110,1110"

ii) ILLUSTRATION

I/O(=DQ)		31 24	23 16	15 8	7 0
DQMi		DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	White DQ24=H	White DQ16=H	White DQ8=H	White DQ0=L
	001	White DQ25=H	White DQ17=H	White DQ9=L	White DQ1=H
	010	White DQ26=H	White DQ18=L	White DQ10=H	White DQ2=H
	011	White DQ27=L	White DQ19=H	White DQ11=H	White DQ3=H
	100	White DQ28=H	White DQ20=H	White DQ12=H	White DQ4=L
	101	White DQ29=H	White DQ21=H	White DQ13=L	White DQ5=H
	110	White DQ30=H	White DQ22=L	White DQ14=H	White DQ6=H
	111	White DQ31=L	White DQ23=H	White DQ15=H	White DQ7=H
After Block Write	000	Blue	Green	Yellow	White
	001	Blue	Green	White	White
	010	Blue	White	Yellow	White
	011	White	Green	Yellow	White
	100	Blue	Green	Yellow	White
	101	Blue	Green	White	White
	110	Blue	White	Yellow	White
	111	White	Green	Yellow	White

Note 2

* Note : 1. DQM byte masking.

2. At normal write, One column is selected among columns decoded by A2-0 (000-111)

At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

(Continued)

Pixel and I/O masking : By Mask at Write Per Bit Mode, the selected bit planes keep the original data.
By Pixel Data issued through DQ pin, the selected pixels keep the original data.
See PIXEL TO DQ MAPPING TANLE.

Assume 8bpp,
White = "0000,0000", Red = "1010,0011", Green = "1110,0001", Yellow = "0000,1111", Blue = "1100,0011"

i) STEP
•• SMRS (LCR) : Load color (for 8bpp, through X 32 DQ color0-3 are loaded into color registers)
Load (color3, color2, color1, color0) = (Blue, Green, Yellow, Red)
= "1100,0011,1110,0001,0000,1111,1010,0011"
••SMRS (LMR) : Load mask, Mask[31-0] = "1111,1111,1101,1101,0100,0010,0111,0110"
→ Byte 3:No I/O Masking; Byte 2:I/O Masking; Byte 1:I/O and Pixel Masking; Byte 0:DQM Byte Masking
•• Row Active with DSF "H" : I/O Mask by Write Per Bit Mode Enable
•• Block Write with DQ[31-0] = "0111,0111,1111,1111,0101,0101,1110,1110"   (Pixel Mask)

ii) ILLUSTRATUON

I/O(=DQ)	31 24	23 16	15 8	7 0
Color Register	Blue	Green	Yellow	Red
	1 1 0 0 0 0 1 1	1 1 1 0 0 0 0 1	0 0 0 0 1 1 1 1	1 0 1 0 0 0 1 1
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	1 1 1 1 1 1 1 1	1 1 0 1 1 1 0 1	0 1 0 0 0 0 1 0	0 1 1 1 0 1 1 0
Before Write	Yellow	Yellow	Green	White
	0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1	1 1 1 0 0 0 0 1	0 0 0 0 0 0 0 0
After Write	Blue	Blue	Red	White
	1 1 0 0 0 0 1 1	1 1 0 0 0 0 1 1	1 0 1 0 0 0 1 1	0 0 0 0 0 0 0 0

Note 1

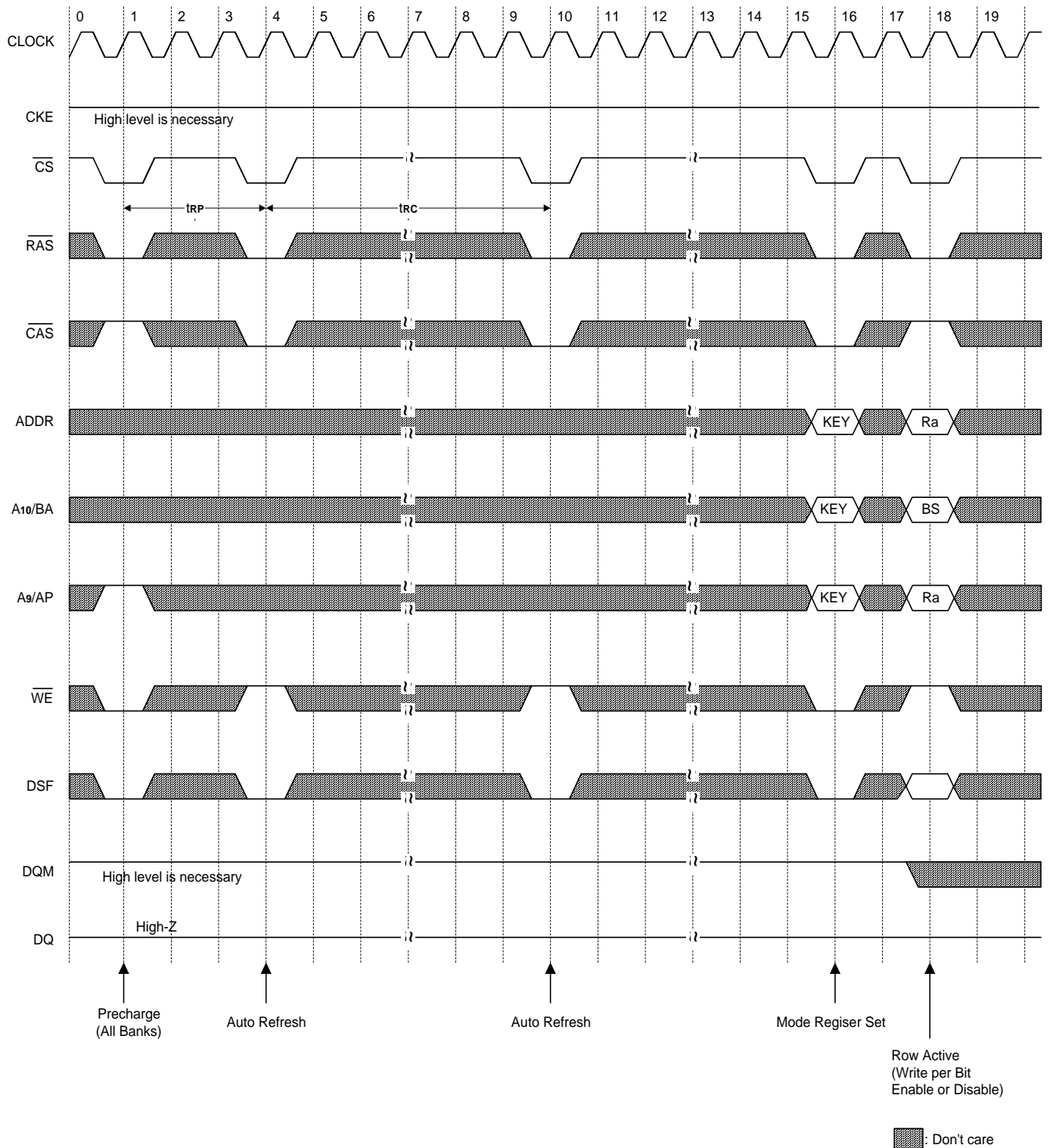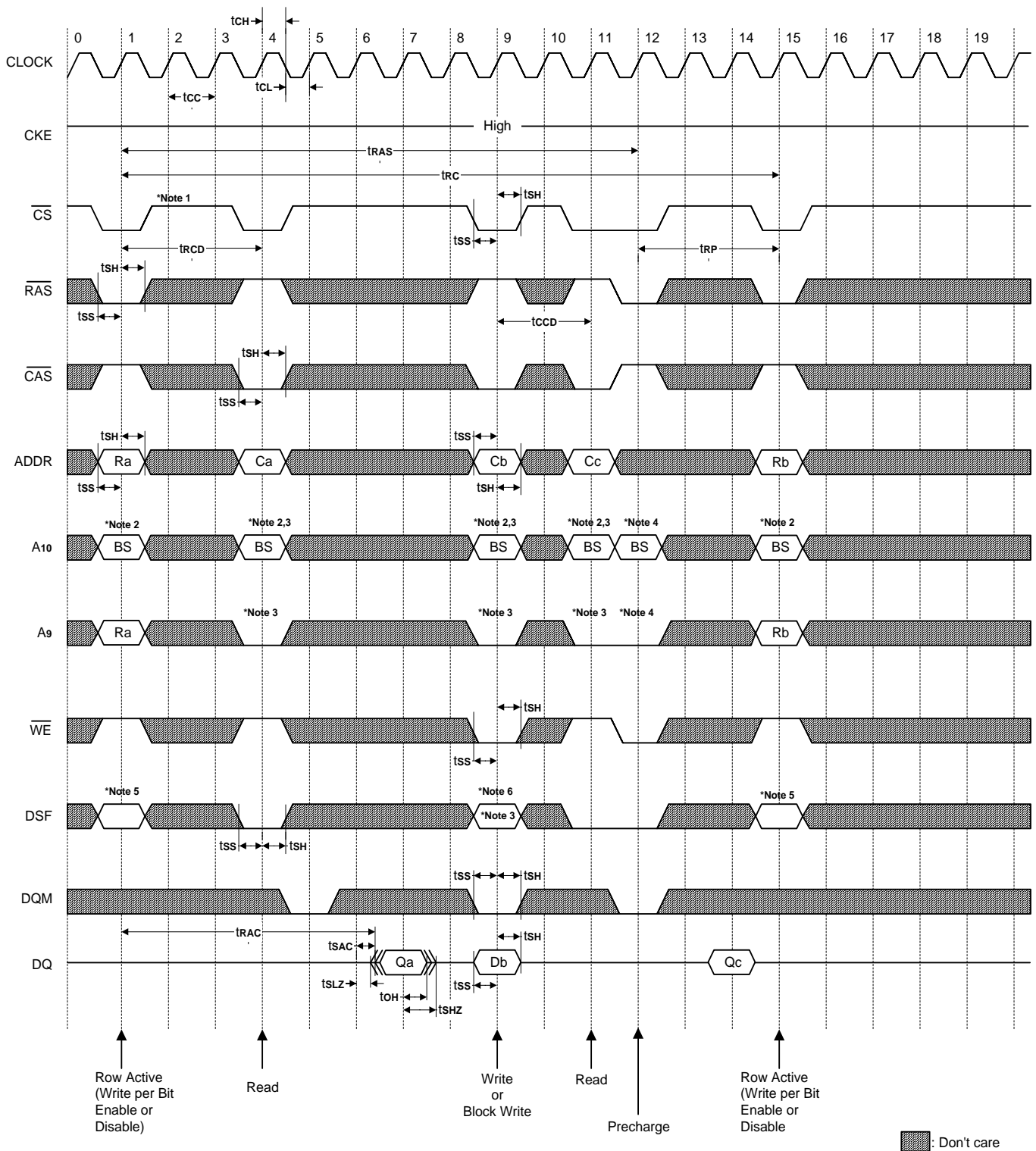| I/O(=DQ)		31 24	23 16	15 8	7 0
DQMi		DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register		Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)	000	Yellow DQ24=H	Yellow DQ16=H	Green DQ8=H	White DQ0=L
	001	Yellow DQ25=H	Yellow DQ17=H	Green DQ9=L	White DQ1=H
	010	Yellow DQ26=H	Yellow DQ18=H	Green DQ10=H	White DQ2=H
	011	Yellow DQ27=L	Yellow DQ19=H	Green DQ11=H	White DQ3=H
	100	Yellow DQ28=H	Yellow DQ20=H	Green DQ12=H	White DQ4=L
	101	Yellow DQ29=H	Yellow DQ21=H	Green DQ13=L	White DQ5=H
	110	Yellow DQ30=H	Yellow DQ22=H	Green DQ14=H	White DQ6=H
	111	Yellow DQ31=L	Yellow DQ23=H	Green DQ15=L	White DQ7=H
After Block Write	000	Blue	**Blue**	**Red**	White
	001	Blue	**Blue**	Green	White
	010	Blue	**Blue**	**Red**	White
	011	Yellow	**Blue**	Green	White
	100	Blue	**Blue**	**Red**	White
	101	Blue	**Blue**	Green	White
	110	Blue	**Blue**	**Red**	White
	111	Yellow	**Blue**	Green	White
		Note 2			Note 1
		PIXEL MASK	I/O MASK	PIXEL & I/O MASK	BYTE MASK

* Note : 1. DQM byte masking.
2. At normal write, One column is selected among columns decoded by A2-0 (000-111)
At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

Power On Sequence & Auto Refresh

CLOCK

CKE — High level is necessary

CS̄

RAS̄ — tRP — tRC

CAS̄

ADDR — KEY — Ra

A10/BA — KEY — BS

A9/AP — KEY — Ra

WĒ

DSF

DQM — High level is necessary

DQ — High-Z

Precharge (All Banks)

Auto Refresh

Auto Refresh

Mode Regiser Set

Row Active (Write per Bit Enable or Disable)

▨ : Don't care

Single Bit Read-Write-Read Cycles (Same Page) @CAS Latency=3, Burst Length=1

* Note : 1. All inputs can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by A10.

A10	Active & Read/Write
0	Bank A
1	Bank B

3. Enable and disable auto precharge function are controlled by A9 in read/write command.

A9	A10	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

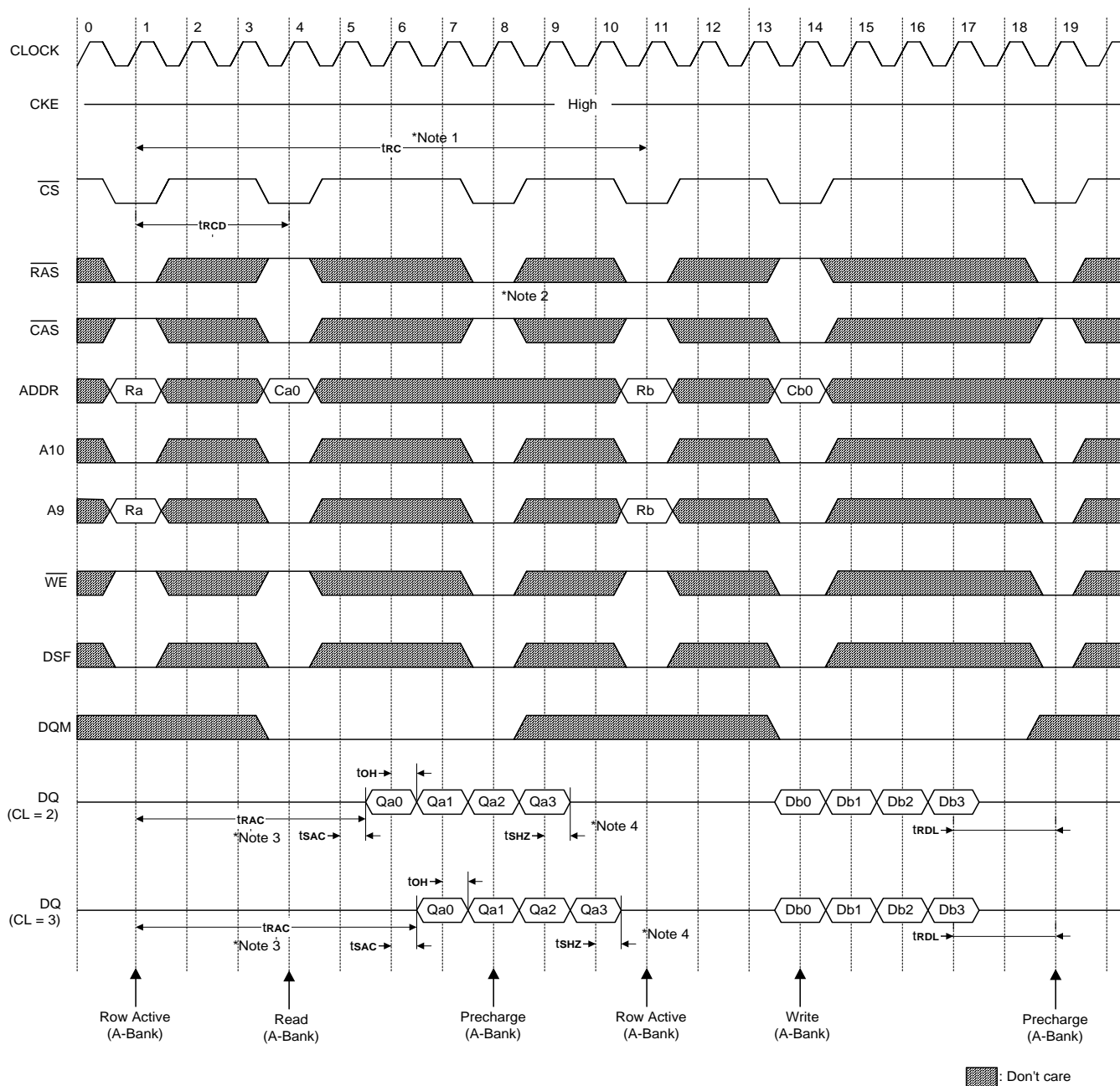4. A9 and A10 control bank precharge when precharge command is asserted.

A9	A10	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Bank

5. Enable and disable Write-per Bit function are controlled by DSF in Row Active command.

A10	DSF	Operation
0	L	Bank A row active, disable write per bit function for bank A
	H	Bank A row active, enable write per bit function for bank A
1	L	Bank B row active, disable write per bit function for bank B
	H	Bank B row active, enable write per bit function for bank B

6. Block write/normal write is controlled by DSF

DSF	Operation	Minimum cycle time
L	Normal write	t_{CCD}
H	Block write	t_{BWC}

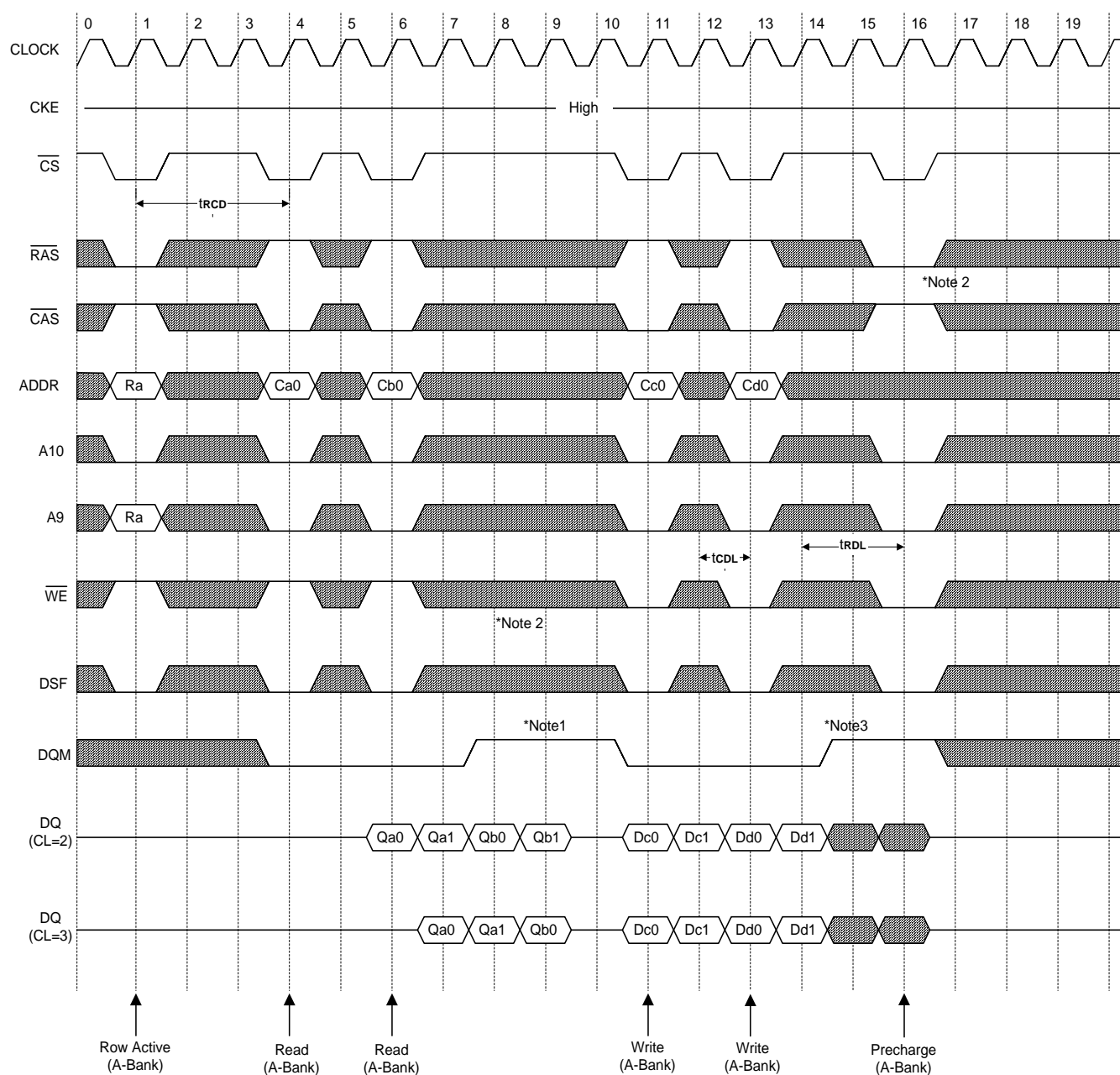## Read & Write Cycle at Same Bank @Burst Length=4

*Note : 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS latency-1] valid output data available after Row enters precharge. Last valid output will be Hi-Z after t_{SHZ} from the clock.

3. Access time from Row address. t_{CC}*(t_{RCD} + CAS latency-1) + t_{SAC}

4. Output will be Hi-Z after the end of burst. (1,2,4 & 8)
   At Full page bit burst, burst is wrap-around.

Page Read & Write Cycle at Same Bank @Burst Length=4

Row Active (A-Bank) ... Read (A-Bank) ... Read (A-Bank) ... Write (A-Bank) ... Write (A-Bank) ... Precharge (A-Bank)

: Don't care

*Note : 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t$_{RDL}$ before Row precharge, will be written.

3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Block Write Cycle (with Auto Precharge)

CLOCK 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
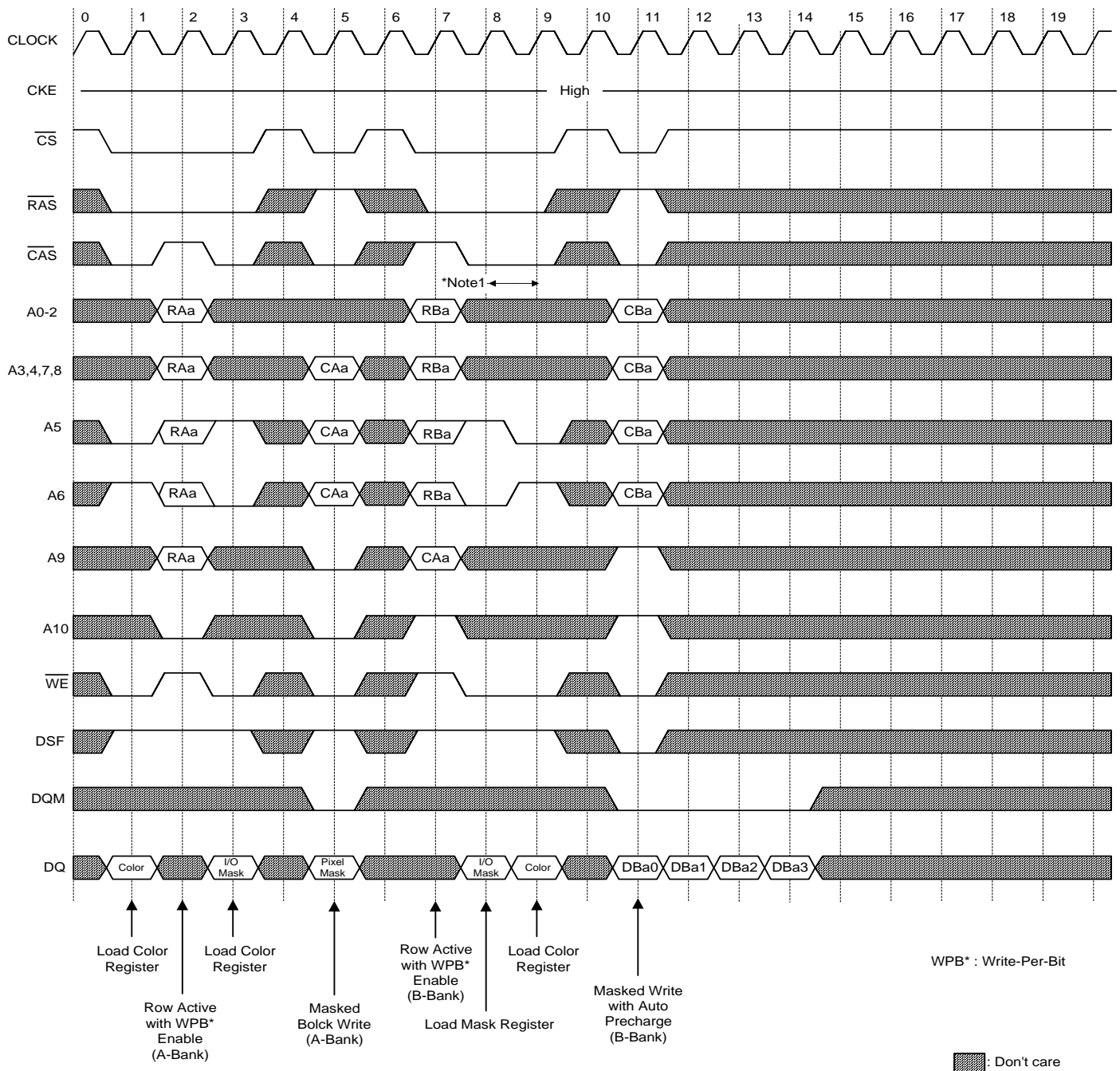
CKE — High

CS

RAS

CAS

*Note 2
ADDR — RAa — CAa — CAb — RBa — CBa — CBb

A10

A9 — RAa — RBa

WE

DSF

tBWC

DQM

*Note 1
DQ — Pixel Mask — Pixel Mask — Pixel Mask — Pixel Mask

Row Active with
Write-per-Bit
Enable
(A-Bank)

Masked
Block Write
(A-Bank)

Masked
Block Write with
Auto Precharge
(A-Bank)

Row Active
(B-Bank)

Block Write
(B-Bank)

Block Write with
Auto Precharge
(B-Bank)

: Don't care
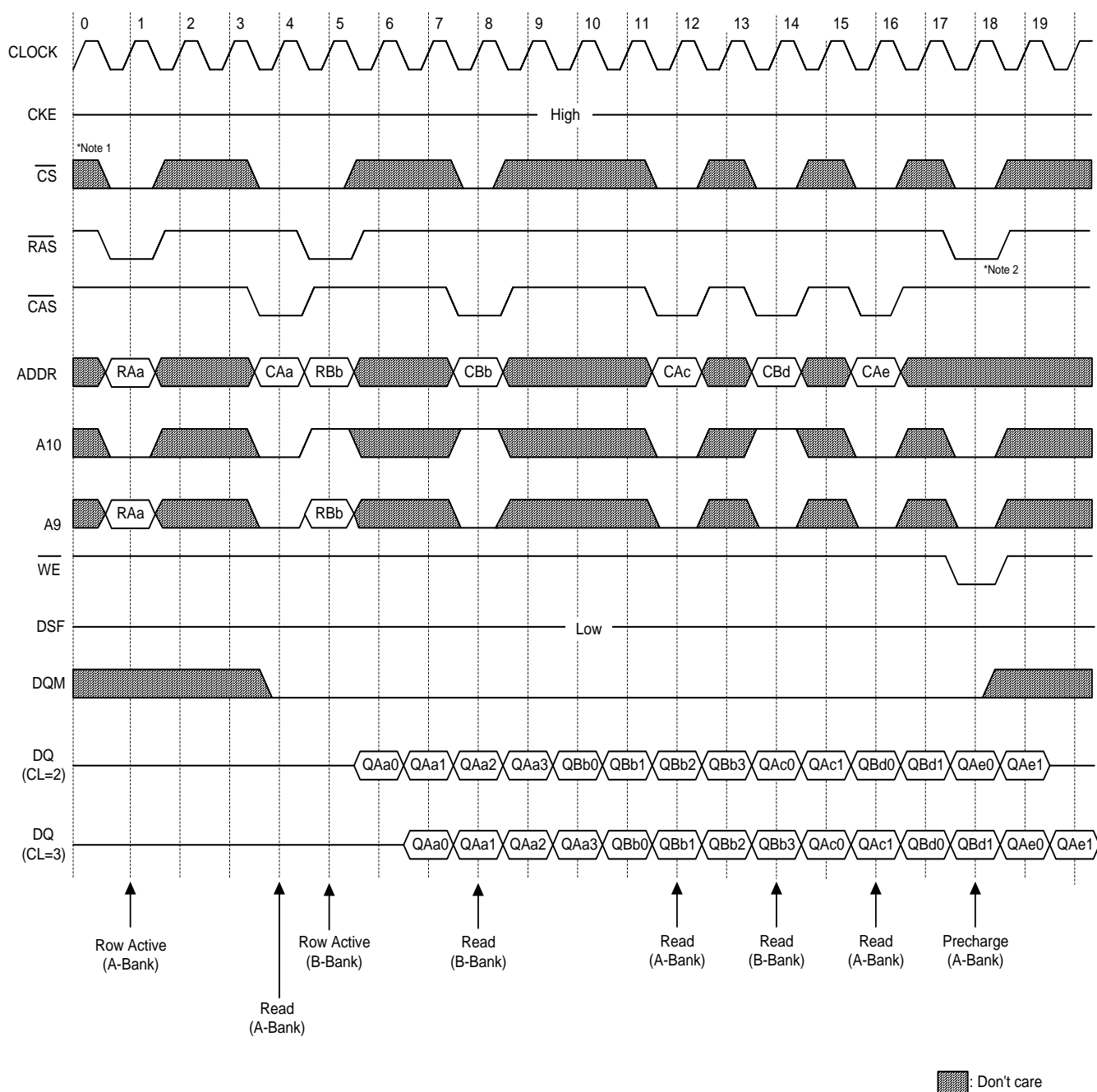
*Note : 1. Column Mask (DQi=L : Mask, DQi=H : Non Mask)

2. At Block Write, CA0-2 are ignored.

SMRS and Block/Normal Write @ Burst Length=4

* Note : 1. At the next clock of special mode set command, new command is possible.

Page Read Cycle at Different Bank @Burst Length = 4

: Don't care

* Note : 1. $\overline{CS}$ can be don't care when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.

2. To interrupt a burst read by row precharge, both the read ad the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4

Row Active with
Write-Per-Bit
enable
(A-Bank)

Load Mask
Register

Masked Write
(A-Bank)

Row Active
(B-Bank)

Write
(B-Bank)

Masked Write
with auto
precharge
(A-Bank)

Write with auto
Precharge
(B-Bank)

: Don't care

Read & Write Cycle at Different Bank @Burst Length=4

* Note : 1. t**CDL** should be met to complete write.

Read & Write Cycle with Auto Precharge I @Burst Length=4

Row Active
(A-Bank)

Row Active
(B-Bank)

Read with
Auto Precharge
(A-Bank)

Auto Precharge
Start Point
(A-Bank)

Write with
Auto Precharge
(B-Bank)

Auto Precharge
Start Point
(B-Bank)

: Don't care

*Note : 1. tRCD should be controlled to meet minimum tRAS before internal precharge start.

(In the case of Burst Length=1 & 2, BRSW mode and Block write)

Read & Write Cycle with Auto Precharge II @Burst Length=4

Row Active
(A-Bank)

Row Active
(B-Bank)

Read with
Auto Pre
Charge
(A-Bank)

Read without
Auto Precharge
(B-Bank)
Auto Precharge
Strart Point
(A-Bank) *Note 1

Precharge
(B-Bank)

Row Active
(A-Bank)

Write with
Auto Precharge
(A-Bank)

: Don't care

* Note : 1. When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.

    - if read(Write) command without auto precharge is issued at B-Bank before A Bank auto precharge starts, A Bank
      auto precharge will start at B Bank read command input point.

    - Any command can not be issued at A Bank during t_{RP} after A Bank auto precharge starts.

Read & Write Cycle with Auto Precharge III @Burst Length=4

Row Active
(A-Bank)

Read with
Auto Preharge
(A-Bank)

Auto Precharge
Start Point
(A-Bank)
Row Active
(B-Bank)

Read with
Auto Precharge
(B-Bank)

Auto Precharge
Start Point
(B-Bank)

* Note 1

: Don't care

* Note : 1. Any command to A-bank is not allowed in this period.

tRP is determined from at auto precharge start point

Read Interrupted by Precharge Command & Read Burst Stop Cycle (@Full Page Only)

: Don't care

* Note : 1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.

2. About the valid DQ's after burst stop, it is same as the case of $\overline{RAS}$ interrupt.

    Both cases are illustrated above timing diagram. See the label 1,2 on them.

    But at burst write, burst stop and $\overline{RAS}$ interrupt should be compared carefully.

    Refer the timing diagram of "Full page write burst stop cycle".

Write Interrupted by Precharge Command & Write Burst Stop Cycle (@ Full Page Only)

| CLOCK | 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 |

CKE .... High ....

Signals: CS, RAS, CAS, ADDR (RAa, CAa, CAb), A10 (* Note 1), A9 (RAa), WE (tBDL, tRDL), DSF, DQM (* Note 3), DQ (* Note 2, DAa0 DAa1 DAa2 DAa3 DAa4, DAb0 DAb1 DAb2 DAb3 DAb4 DAb5)

Row Active (A-Bank) — Write (A-Bank) — Burst Stop — Write (A-Bank) — Precharge (A-Bank)
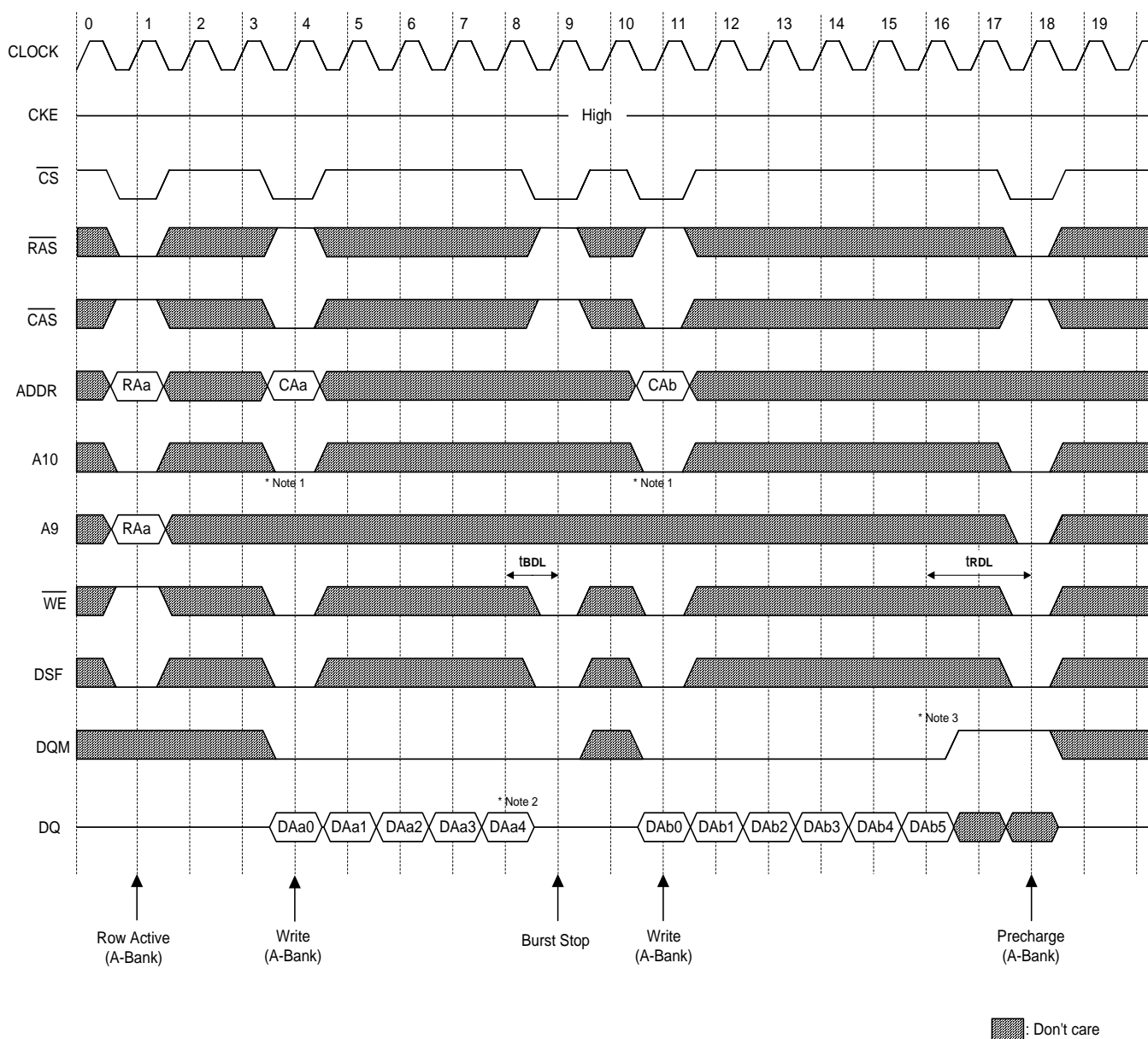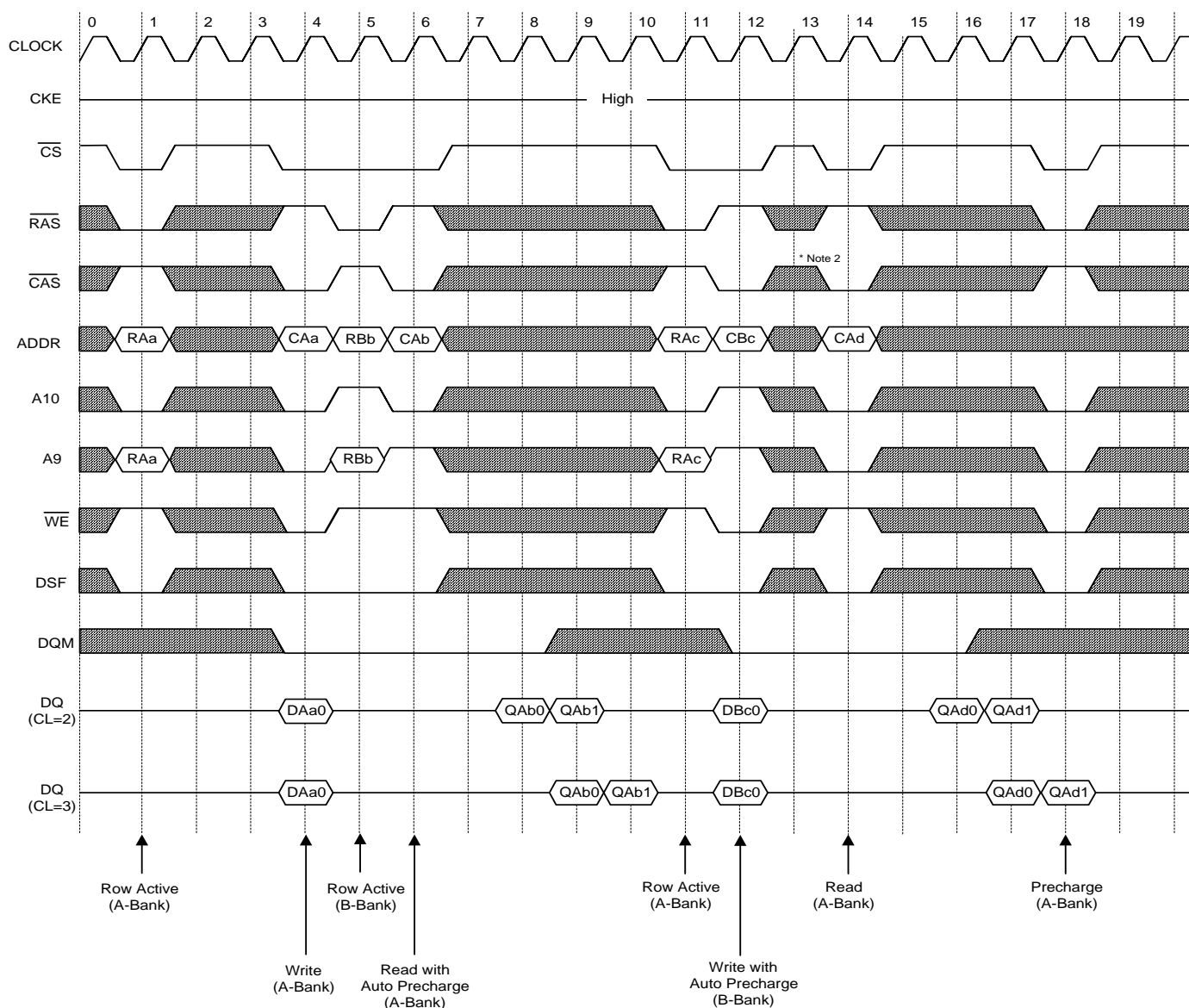
: Don't care

* Note : 1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.

      2. Data-in at the cycle of burst stop command cannot be written into corresponding memory cell.

         It is defined by AC parameter of tBDL(=1CLK).

      3. Data-in at the cycle of interrupted by precharge cannot be written into the corresponding memory cell.

         It is defined by AC parameter of tRDL(2=CLK).

         DQM at write interrupted by precharge command is needed to ensure tRDL of 2CLK.

         DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst.

         Input data after Row precharge cycle will be masked internally.

      4. Burst stop is valid only at full page burst length.

Burst Read Single Bit Write Cycle @Burst Length=2, BRSW

: Don't care

* Note : 1. BRSW mode is enabled by setting A9 "High" at MRS (Mode Register Set).

At the BRSW Mode, the burst length at write is fixed to "1" regardless of programed burst length.

2. When BRSW write command with auto precharge is executed, keep it in mind that tRAS should not be violated.

Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,

The next cycle starts the precharge.

3. WPB function is also possible at BRSW mode.

Clock Suspension & DQM Operation Cycle @CAS Latency = 2, Burst Length=4

: Don't care

* Note : 1. DQM needed to prevent bus contention.

Active/Precharge Power Down Mode @CAS Lantency=2, Burst Length=4

Precharge
Power-down
Entry

Precharge
Power-down
Exit

Row Active

Active
Power-down
Entry

Active
Power-down
Exit

Read

Precharge

: Don't care

* Note : 1. All banks should be in idle state prior to entering precharge power down mode.

2. CKE should be set high at least "1CLK + tss" prior to Row active command.

3. Cannot violate minimum refresh specification. (32ms)

Self Refresh Entry & Exit Cycle

Self Refresh Entry

Self Refresh Exit

Auto Refresh

: Don't care

* Note : TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.

2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.

3. The device remains in self refresh mode as long as CKE stays "Low".

   (cf.) Once the device enters self refresh mode, minimum tRAS is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.

5. $\overline{CS}$ starts from high.

6. Minimum tRC is required after CKE going high to complete self refresh exit.

7. 2K cycle of burst auto refresh is required before self refresh entry and after self refresh exit.

   If the system uses burst refresh.

Mode Register Set Cycle   **Auto Refresh Cycle**

: Don't care

* Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

* Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation and DSF of low at the same clock cycle with address key will set internal mode register.

2. Minimum 1 clock cycles should be met before new $\overline{RAS}$ activation.

3. Please refer to Mode Register Set table.

Function Truth Table (Table 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	Address	Action	Note
IDLE	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	X	X	BA	CA	ILLEGAL	2
	L	L	H	H	L	BA	RA	Row Active; Latch Row Address; Non-IO Mask	
	L	L	H	H	H	BA	RA	Row Active; latch Row Address; IO Mask	
	L	L	H	L	L	BA	PA	NOP	4
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	H	L	X	X	Auto Refresh or Self Refresh	5
	L	L	L	H	H	X	X	ILLEGAL	
	L	L	L	L	L	OP Code		Mode Register Access	5
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Row Active	H	X	X	X	X	X	X	NOP	
	L	H	H	H	X	X	X	NOP	
	L	H	H	L	X	X	X	ILLEGAL	2
	L	H	L	H	L	BA	CA,AP	Begin Read; Latch CA; Determine AP	
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Begin Write; Latch CA; Determine AP	
	L	H	L	L	H	BA	CA,AP	Block Write; Latch CA; Determine AP	
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Precharge	
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	H	X	X	X	ILLEGAL	
	L	L	L	L	L	X	X	ILLEGAL	
	L	L	L	L	H	OP Code		Special Mode Register Access	6
Read	H	X	X	X	X	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	L	L	X	X	Term burst →Row Active	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA,AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Term burst; Begin Write; Latch CA; Determine AP	3
	L	H	L	L	H	BA	CA,AP	Term burst; Block Write; Latch CA; Determine AP	3
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Term Burst; Precharge timing for Reads	3
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	

Function Truth Table (Table 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	Address	Action	Note
Write	H	X	X	X	X	X	X	NOP(Continue Burst to End→Row Active)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End→Row Active)	
	L	H	H	L	L	X	X	Term burst →Row Active)	
	L	H	H	L	H	X	X	ILLEGAL	
	L	H	L	H	L	BA	CA,AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	H	H	X	X	ILLEGAL	
	L	H	L	L	L	BA	CA,AP	Term burst; Begin Write; Latch CA; Determine AP	3
	L	H	L	L	H	BA	CA,AP	Term burst; Block Write; Latch CA; Determine AP	3
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	L	BA	PA	Term Burst; Precharge timing for Writes	3
	L	L	H	L	H	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA,AP	ILLEGAL	2
	L	H	L	L	X	BA	CA,AP	ILLEGAL	2
	L	L	H	X	X	BA	RA,PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Write with Auto Precharge	H	X	X	X	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	H	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	H	X	BA	CA,AP	ILLEGAL	2
	L	H	L	L	X	BA	CA,AP	ILLEGAL	2
	L	L	H	X	X	BA	RA,PA	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	2
Precharge	H	X	X	X	X	X	X	NOP→Idle after t$_{RP}$	
	L	H	H	H	X	X	X	NOP→Idle after t$_{RP}$	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	NOP→Idle after t$_{RP}$	2
	L	L	L	X	X	X	X	ILLEGAL	4
Block Write Recovering	H	X	X	X	X	X	X	NOP→Row Active after t$_{BWC}$	
	L	H	H	H	X	X	X	NOP→Row Active after t$_{BWC}$	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	Term Block Write: Precharge timing for Block Write	2
	L	L	L	X	X	X	X	ILLEGAL	2

Function Truth Table (Table 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	Address	Action	Note
Row Activating	H	X	X	X	X	X	X	NOP→Row Active after t$_{RCD}$	
	L	H	H	H	X	X	X	NOP→Row Active after t$_{RCD}$	
	L	H	H	L	X	X	X	ILLEGAL	
	L	H	L	X	X	BA	CA,AP	ILLEGAL	2
	L	L	H	H	X	BA	RA	ILLEGAL	2
	L	L	H	L	X	BA	PA	ILLEGAL	2
	L	L	L	X	X	X	X	ILLEGAL	2
Refreshing	H	X	X	X	X	X	X	NOP→Idle after t$_{RC}$	
	L	H	H	X	X	X	X	NOP→Idle after t$_{RC}$	
	L	H	L	X	X	X	X	ILLEGAL	
	L	L	H	X	X	X	X	ILLEGAL	
	L	L	L	X	X	X	X	ILLEGAL	

Abbreviations

RA = Row Address (A0~A9) BA = Bank Address (A10) PA = Precharge All (A9)
NOP = No Operation Command CA = Column Address (A0~A7) AP = Auto Precharge (A9)

Note: 1. All entries assume that CKE was active (High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state : Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and PA).
5. Illegal if any bank is not idle.
6. Legal only if all banks are in idle or row active state.

Function Truth Table for CKE (Table 2)

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Self Refresh	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Self Refresh→ABI after t$_{RC}$	7
	L	H	L	H	H	H	X	X	Exit Self Refresh→ABI after t$_{RC}$	7
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP (Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	X	Exit Power Down→ABI	8
	L	H	L	H	H	H	X	X	Exit Power Down→ABI	8
	L	H	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	L	X	X	X	ILLEGAL	
	L	H	L	L	X	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP(Maintain Power Down Mode)	
All Banks Idle	H	H	X	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	X	Enter Power Down	9
	H	L	L	H	H	H	X	X	Enter Power Down	9
	H	L	L	H	H	L	X	X	ILLEGAL	
	H	L	L	H	L	X	X	X	ILLEGAL	
	H	L	L	L	H	X	X	X	ILLEGAL	
	H	L	L	L	L	H	L	X	Enter Self Refresh	9
	H	L	L	L	L	L	X	X	ILLEGAL	
	L	L	X	X	X	X	X	X	NOP	
Any State Other than Listed Above	H	H	X	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	10
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	10
	L	L	X	X	X	X	X	X	Maintain clock Suspend	

Abbreviations : ABI = All Banks Idle

Note: 7. After CKE's low to high transition to exit self refresh mode. And a time of t$_{RC}$(min) has to be elapse after CKE's low to high transition to issue a new command.
8. CKE low to high transition is asynchronous as if restarts internal clock.
A minimum setup time "t$_{SS}$ + one clock" must be satisfied before any command other than exit.
9. Power-down and self refresh can be entered only from the all banks idle state.
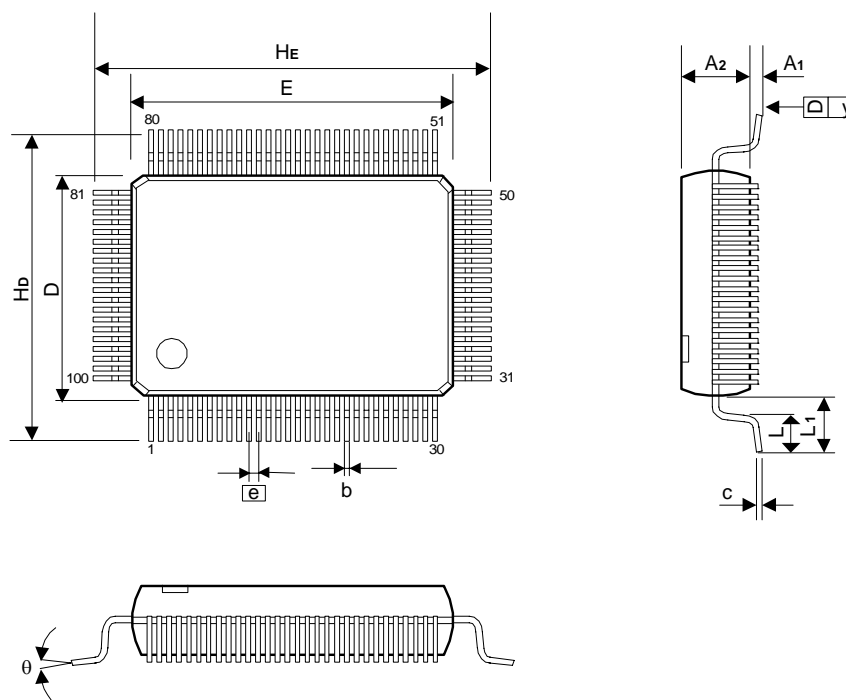10. Must be a legal command.

Ordering Information

Part No.	Cycle Time (ns)	Clock Frequency (MHz)	Access Time	Package
A45L9332AF-6		166	5.5 ns @ CL = 3	100 QFP
A45L9332AF-6F	6	166	5.5 ns @ CL = 3	100 Pb-Free QFP
A45L9332AE-6		166	5.5 ns @ CL = 3	100 LQFP
A45L9332AE-6F		166	5.5 ns @ CL = 3	100 Pb-Free LQFP
A45L9332AF-7		143	6.0 ns @ CL = 3	100 QFP
A45L9332AF-7F	7	143	6.0 ns @ CL = 3	100 Pb-Free QFP
A45L9332AE-7		143	6.0 ns @ CL = 3	100 LQFP
A45L9332AE-7F		143	6.0 ns @ CL = 3	100 Pb-Free LQFP
A45L9332AF-8		125	6.5 ns @ CL = 3	100 QFP
A45L9332AF-8F	8	125	6.5 ns @ CL = 3	100 Pb-Free QFP
A45L9332AE-8		125	6.5 ns @ CL = 3	100 LQFP
A45L9332AE-8F		125	6.5 ns @ CL = 3	100 Pb-Free LQFP

* QFP (Height = 3.0mm Max)

  LQFP (Height = 1.4mm Max)

Package Information

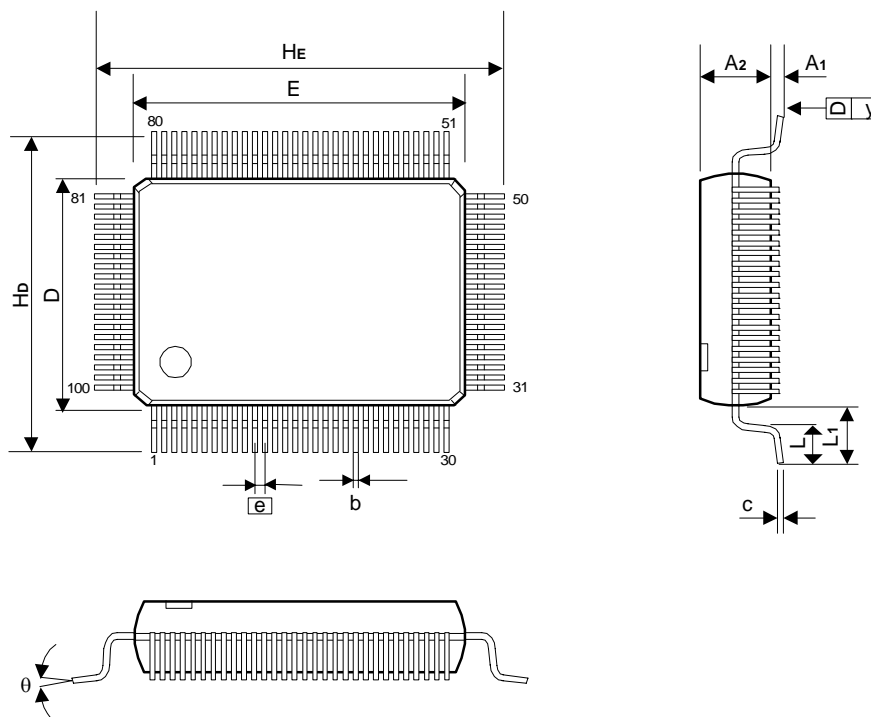**QFP 100L Outline Dimensions**   unit: inches/mm

Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.004	-	-	0.100	-	-
A2	0.107	0.112	0.117	2.723	2.85	2.977
b	0.010	-	0.014	0.26	-	0.36
c	0.0057	0.006	0.0063	0.142	0.150	0.158
HE	0.905	0.913	0.921	22.950	23.200	23.450
E	0.783	0.787	0.791	19.900	20.000	20.100
HD	0.669	0.677	0.685	16.950	17.200	17.450
D	0.547	0.551	0.555	13.900	14.000	14.100
e	0.020	0.026	0.032	0.500	0.650	0.800
L	0.025	0.031	0.037	0.650	0.800	0.950
L1	0.057	0.063	0.069	1.450	1.600	1.750
y	-	-	0.004	-	-	0.100
θ	0°	-	8°	0°	-	8°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.

Package Information

LQFP 100L Outline Dimensions   unit: inches/mm

Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A$_1$	0.002	-	-	0.05	-	-
A$_2$	0.053	0.055	0.057	1.35	1.40	1.45
b	0.011	0.013	0.015	0.27	0.32	0.37
c	0.005	-	0.008	0.12	-	0.20
H$_E$	0.860	0.866	0.872	21.85	22.00	22.15
E	0.783	0.787	0.791	19.90	20.00	20.10
H$_D$	0.624	0.630	0.636	15.85	16.00	16.15
D	0.547	0.551	0.555	13.90	14.00	14.10
e	0.026 BSC			0.65 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L$_1$	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.1
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.