DATA SHEET

TDA5051
Home automation modem

Product specification
Supersedes data of 1997 Mar 11
File under Integrated Circuits, IC11

1997 Sep 19

Philips
Semiconductors

PHILIPS

Home automation modem TDA5051

FEATURES

- Full digital carrier generation and shaping
- Modulation/demodulation frequency set by clock adjustment, from microcontroller or on-chip oscillator
- High clock rate of 6 bits D/A (Digital-to-Analog) converter for rejection of aliasing components
- Fully integrated output power stage with overload protection
- Automatic gain control at receiver input
- 8-bit A/D and narrow digital filtering
- Digital demodulation delivering baseband data
- Easy compliance with EN50065-1 with simple coupling network
- Few external components for low cost applications
- SO16 plastic package.

APPLICATIONS

- Home appliance control (air conditioning, shutters, lighting, alarms and so on)
- Energy/heating control
- ASK (Amplitude Shift Keying) data transmission using the home power network.

GENERAL DESCRIPTION

The TDA5051 is a modem IC, specifically dedicated to ASK transmission by means of the home power supply network, at 600 or 1200 baud data rate. It operates from a single 5 V supply.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	f_{osc} = 8.48 MHz				
	reception mode		–	28	38	mA
	transmission mode ($\overline{DATA}_{IN}$ = 0)	Z_L = 30 Ω	–	47	68	mA
	power down mode		–	19	25	mA
T_{amb}	operating ambient temperature		0	–	70	°C
f_{cr}	carrier frequency	note 1	95	132.5	148.5	kHz
f_{osc}	oscillator frequency		6.08	8.48	9.504	MHz
$V_{o(rms)}$	output carrier signal on CISPR16 load (RMS value)		120	–	122	dBμV
$V_{i(rms)}$	input signal (RMS value)		66	–	122	dBμV
THD	total harmonic distortion on CISPR16 load with coupling network		–	–55	–	dB
Z_L	load impedance		1	30	–	Ω
BR	baud rate		–	600	1200	bits/s

Note

1. Frequency range corresponding to the EN50065-1 band. However the modem can operate at any lower oscillator frequency.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5051T	SO16	plastic small outline package: 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

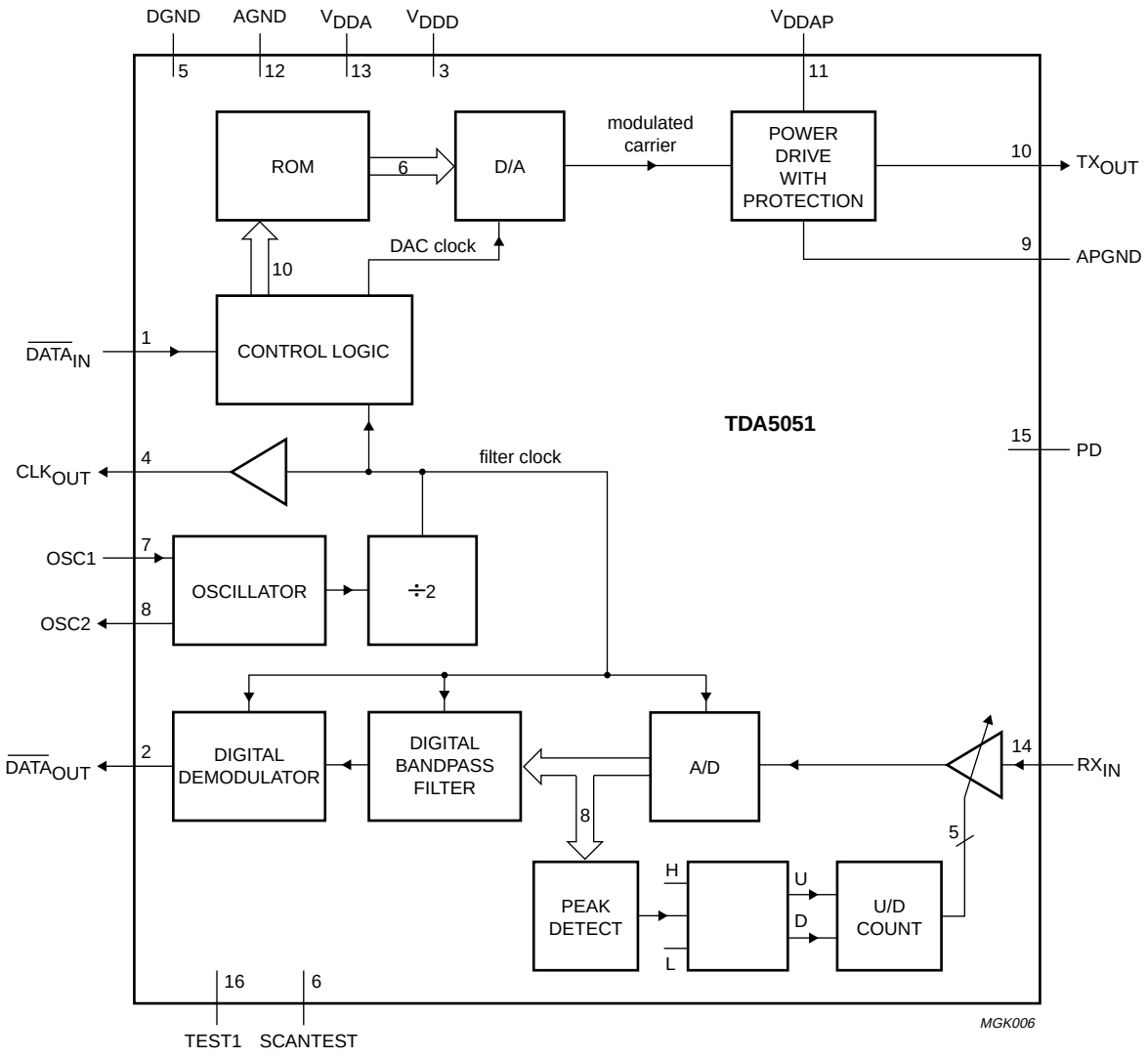


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{DATA}_{IN}$	1	digital data input (active LOW)
$\overline{DATA}_{OUT}$	2	digital data output (active LOW)
V_{DDD}	3	digital supply voltage
CLK_{OUT}	4	clock output
DGND	5	digital ground
SCANTEST	6	test input (LOW in application)
OSC1	7	oscillator input
OSC2	8	oscillator output
APGND	9	analog ground for power amplifier
TX_{OUT}	10	analog signal output
V_{DDAP}	11	analog supply voltage for power amplifier
AGND	12	analog ground
V_{DDA}	13	analog supply voltage
RX_{IN}	14	analog signal input
PD	15	power-down input (active HIGH)
TEST1	16	test input (HIGH in application)

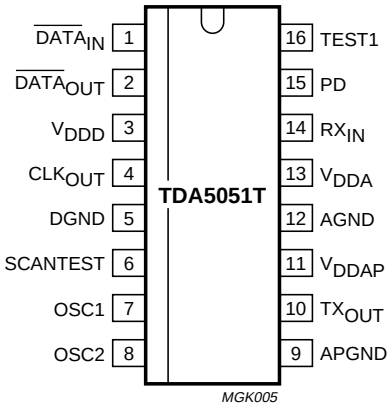


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Both transmission and reception stages are controlled either by the master clock of the microcontroller, or by the on-chip reference oscillator connected to a crystal. This holds for the accuracy of the transmission carrier and the exact trimming of the digital filter, thus making the performance totally independent of application disturbances such as component spread, temperature, supply drift and so on.

The interface with the power network is made by means of a LC network (see Fig.18). The device includes a power output stage able to feed a 120 dBμV (RMS) signal on a typical 30 Ω load.

To reduce power consumption, the IC is disabled by a power-down input (pin PD): in this mode, the on-chip oscillator remains active and the clock continues to be supplied at pin CLK_{OUT}. For low-power operation in reception mode, this pin can be dynamically controlled by the microcontroller (see Section “Power-down mode”).

When the circuit is connected to an external clock generator (see Fig.6), the clock signal must be applied at pin OSC1 (pin 7); OSC2 (pin 8) must be left open. Use of the on-chip clock circuitry is shown in Fig.7.

All logic inputs and outputs are compatible with TTL/CMOS levels, providing an easy connection to a standard microcontroller I/O port.

The digital part of the IC is fully scan-testable. Two digital inputs, SCANTEST and TEST1, are used for production test: these pins must be left open in functional mode (correct levels are internally defined by pull-up/down resistors).

Transmission mode

The carrier frequency is generated by the scanning of a ROM memory under the control of the microcontroller clock or the reference frequency provided by the on-chip oscillator, thus providing strict stability with respect to environmental conditions. High frequency clocking rejects the aliasing components to such an extent that they are filtered by the coupling LC network and do not cause any significant disturbance. The data modulation is applied through pin $\overline{DATA}_{IN}$ and smoothly applied by specific digital circuitry to the carrier (shaping). Harmonic components are limited in this process, thus avoiding unacceptable disturbance of the transmission channel (according to CISPR16 and EN50065-1 recommendations). A –55 dB total harmonic distortion is reached when using the typical LC coupling network (or an equivalent filter).

The D/A converter and the power stage are set in order to provide a maximum signal level of 122 dBμV (RMS) at the output.

The output of the power stage (TX_{OUT}) **always** has to be connected to a decoupling capacitor, because of a DC level of $0.5V_{DD}$ at this pin, present even when the device is not transmitting. This pin also has to be **protected against overvoltage and negative transient signals**. The DC level of TX_{OUT} can be used to bias an unipolar transient suppressor, as shown in the application diagram (see Fig.18).

Direct connection to the mains is done through a LC network for low-cost applications. However, a HF signal transformer could be used when power-line insulation has to be performed.

CAUTION
In transmission mode, the receiving part of the circuit is **not disabled** and the detection of the transmitted signal is normally performed. In this mode, the gain chosen before the beginning of the transmission is stored, and the **AGC is internally set to –6 dB** as long as $\overline{DATA}_{IN}$ is LOW. Then, the old gain setting is **automatically restored**.

Receiving mode

The input signal received by the modem is applied to a wide range input amplifier with Automatic Gain Control (AGC) (–6 to +30 dB). This is basically for noise performance improvement and signal level adjustment that ensures a maximum sensitivity of the A/D converter. Then an 8 bit A/D conversion is performed, followed by digital bandpass filtering, in order to meet the CISPR normalization and to comply with some additional limitations encountered in current applications. After digital demodulation, the baseband data signal is made available after pulse shaping.

The signal pin (RX_{IN}) is a high-impedance input, which has to be protected and DC decoupled for the same reasons as with pin TX_{OUT}. The high sensitivity (66 dBμV) of this input requires an efficient 50 Hz rejection filter (realized by the LC coupling network) also used as an anti-aliasing filter for the internal digital processing (see Fig.18).

Data format

TRANSMISSION MODE

The data input ($\overline{DATA}_{IN}$) is active LOW: this means that a burst is generated on the line (pin TX_{OUT}) when pin $\overline{DATA}_{IN}$ is LOW.

Pin TX_{OUT} is in high-impedance state as long as the device is not transmitting. Successive logic 1s are treated in a NRZ mode (see pulse shape description in Figs 8 and 9).

RECEIVING MODE

The data output (pin $\overline{DATA}_{OUT}$) is active LOW; this means that the data output is LOW when a burst is received. Pin $\overline{DATA}_{OUT}$ remains LOW as long as a burst is received.

Power-down mode

Power-down input (pin PD) is active HIGH; this means that the power consumption is minimal when pin PD is HIGH. All functions, except clock generation, are disabled then.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.5	V
f_{osc}	oscillator frequency	–	12	MHz
T_{stg}	storage temperature	–50	+150	°C
T_{amb}	operating ambient temperature	–10	+80	°C
T_j	junction temperature	–	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

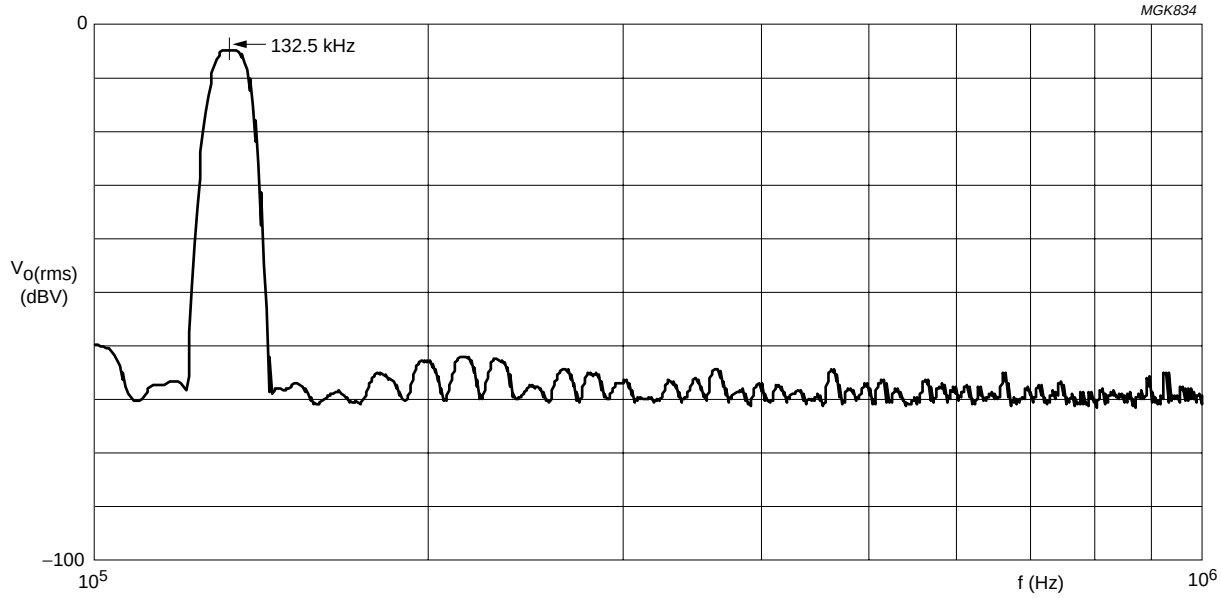
CHARACTERISTICS

$V_{DDD} = V_{DDA} = 5$ V ±5%; $T_{amb} = 0$ to 70 °C; V_{DDD} connected to V_{DDA}; DGND connected to AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.75	5	5.25	V
$I_{DD(RX/TX)(tot)}$	total analog + digital supply current; TX or RX mode	V_{DD} = 5 V ±5%	–	28	38	mA
$I_{DD(PD)(tot)}$	total analog + digital supply current; power-down mode	V_{DD} = 5 V ±5%; PD = HIGH	–	19	25	mA
$I_{DD(PAMP)}$	power amplifier supply current in transmission mode	V_{DD} = 5 V ±5%; Z_L = 30 Ω; $\overline{DATA}_{IN}$ = LOW	–	19	30	mA
$I_{DD(PAMP)(max)}$	maximum power amplifier supply current in transmission mode	V_{DD} = 5 V ±5%; Z_L = 1 Ω; $\overline{DATA}_{IN}$ = LOW	–	76	–	mA
$\overline{DATA}_{IN}$ input, PD input: $\overline{DATA}_{OUT}$ output, CLK_{OUT} output						
V_{IH}	HIGH-level input voltage		$0.2V_{DD}$ + 0.9	–	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DD}$ – 0.1	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1.6 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.45	V
OSC1 input and OSC2 output (OSC2 only used for driving external quartz crystal; must be left open when using an external clock generator)						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	–	$0.2V_{DD}$ – 0.1	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1.6 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.45	V
Clock						
f_{osc}	oscillator frequency		6.080	–	9.504	MHz
$\frac{f_{osc}}{f_{cr}}$	ratio between oscillator and carrier frequency		–	64	–	
$\frac{f_{osc}}{f_{CLKOUT}}$	ratio between oscillator and clock output frequency		–	2	–	

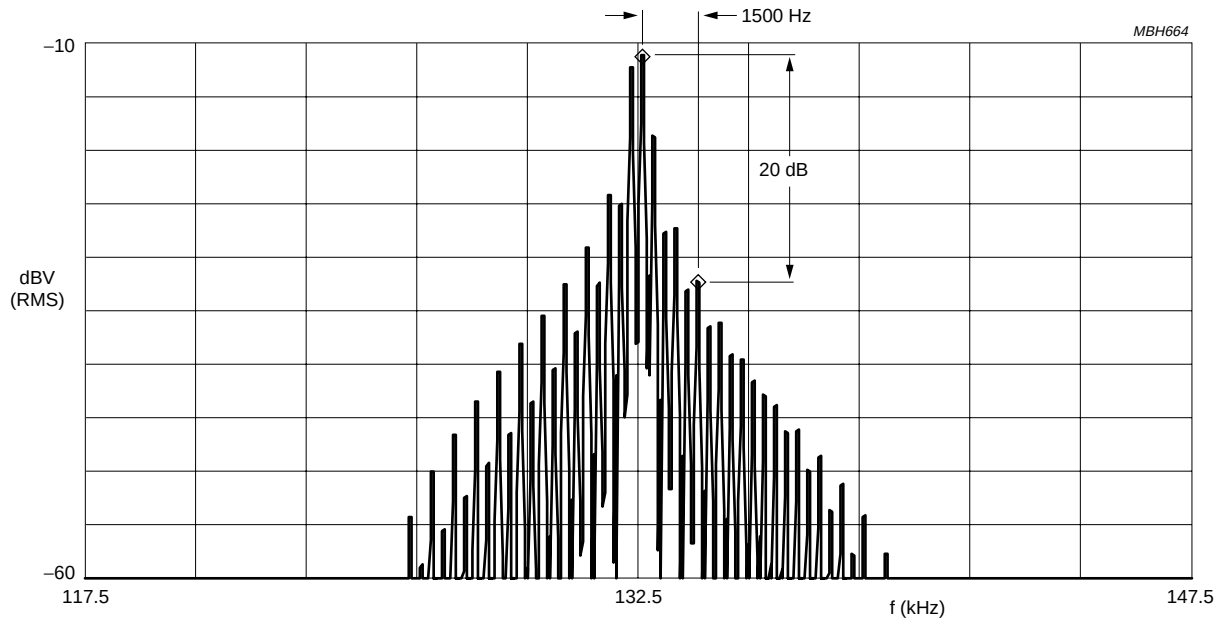
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmission mode						
f_{cr}	carrier frequency	f_{osc} = 8.48 MHz	–	132.5	–	kHz
t_{su}	set-up time of the shaped burst	f_{osc} = 8.48 MHz; see Fig.8	–	170	–	µs
t_h	hold time of the shaped burst	f_{osc} = 8.48 MHz; see Fig.8	–	170	–	µs
$t_{W(DI)(min)}$	minimum pulse width of $\overline{DATA}_{IN}$ signal	f_{osc} = 8.48 MHz; see Fig.8	–	190	–	µs
$V_{o(rms)}$	output carrier signal (RMS value)	Z_L = CISPR16 $\overline{DATA}_{IN}$ = LOW	120	–	122	dBµV
$I_{o(max)}$	power amplifier maximum output current (peak value)	Z_L = 1 Ω; $\overline{DATA}_{IN}$ = LOW	–	160	–	mA
Z_o	output impedance of the power amplifier		–	5	–	Ω
V_O	output DC level at TX_{OUT}		–	2.5	–	V
THD	total harmonic distortion on CISPR16 load with the coupling network (measured on the first ten harmonics)	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{DATA}_{IN}$ = LOW (no modulation); see Figs 3 and 16	–	–55	–	dB
B_{-20dB}	bandwidth of the shaped output signal (at –20 dB) on CISPR16 load with the coupling network	$V_{o(rms)}$ = 121 dBµV on CISPR16 load; f_{osc} = 8.48 MHz; $\overline{DATA}_{IN}$ = 300 Hz; duty factor = 50%; see Fig.4	–	3000	–	Hz
Reception mode						
$V_{i(rms)}$	analog input signal (RMS value)		68	–	122	dBµV
V_I	DC level at pin RX_{IN}		–	2.5	–	V
Z_i	RX_{IN} input impedance		–	50	–	kΩ
R_{AGC}	automatic gain control range		–	36	–	dB
$t_{c(AGC)}$	automatic gain control time constant	f_{osc} = 8.48 MHz; see Fig.5	–	296	–	µs
$t_{d(dem)(su)}$	demodulation delay set-up time	f_{osc} = 8.48 MHz; see Fig.15	–	410	460	µs
$t_{d(dem)(h)}$	demodulation delay hold time	f_{osc} = 8.48 MHz; see Fig.15	–	330	380	µs
B_{det}	detection bandwidth	f_{osc} = 8.48 MHz	–	3	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BER	bit error rate	f_{osc} = 8.48 MHz; 600 baud; S/N = 35 dB; signal 76 dBμV; see Fig.17	–	1	–	1×10^{-4}
Power-up timing						
$t_{d(pu)(TX)}$	delay between power-up and $\overline{DATA}_{IN}$ in transmission mode	XTAL = 8.48 MHz; C1 = C2 = 27 pF; R_p = 2.2 MΩ; see Fig.10	–	1	–	μs
$t_{d(pu)(RX)}$	delay between power-up and $\overline{DATA}_{OUT}$ in reception mode	XTAL = 8.48 MHz; C1 = C2 = 27pF; R_p = 2.2 MΩ; f_{RXIN} = 132.5 kHz; 120 dBμV sinewave; see Fig.11	–	1	–	μs
Power-down timing						
$t_{d(pd)(TX)}$	delay between PD = 0 and $\overline{DATA}_{IN}$ in transmission mode	f_{osc} = 8.48 MHz; see Fig.12	–	10	–	μs
$t_{d(pd)(RX)}$	delay between PD = 0 and $\overline{DATA}_{OUT}$ in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kH; 120 dBμV sinewave; see Fig.13	–	500	–	μs
$t_{active(min)}$	minimum active time with T = 10 ms power-down period in reception mode	f_{osc} = 8.48 MHz; f_{RXIN} = 132.5 kH; 120 dBμV sinewave; see Fig.14	–	1	–	μs



Resolution bandwidth = 9 kHz; top: 0 dBV (RMS) = 120 dBμV (RMS); marker at −5 dBV (RMS) = 115 dBμV (RMS); the CISPR16 network provides an attenuation of 6 dB, so the signal amplitude is 121 dBμV (RMS).

Fig.3 Carrier spectrum.



Resolution bandwidth = 100 Hz; B_{-20dB} = 3000 Hz (2 × 1500 Hz).

Fig.4 Shaped signal spectrum.

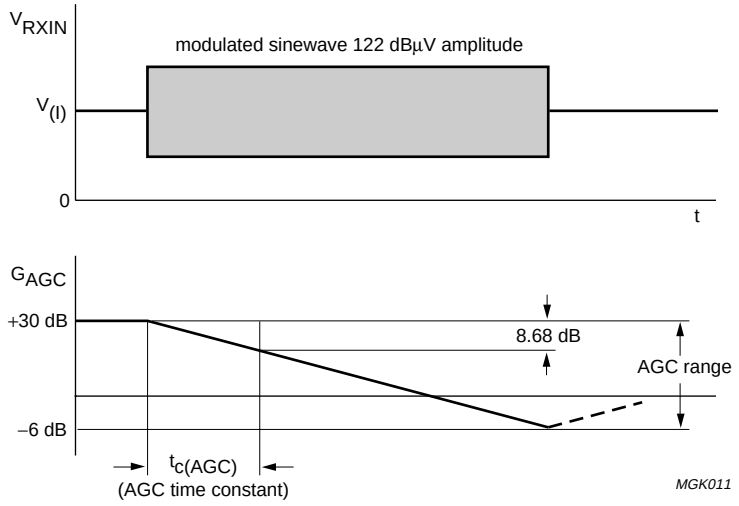
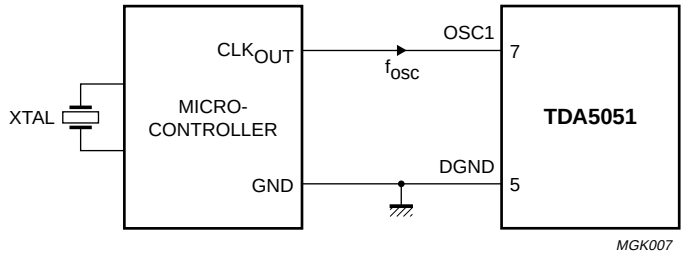


Fig.5 AGC time constant definition (not to scale).

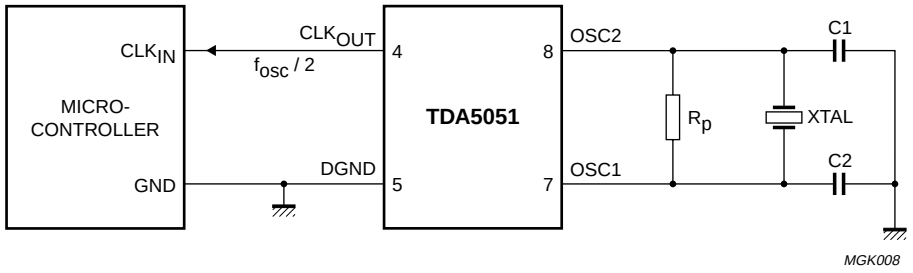
TIMING

Configurations for clock



For parameter description see Table 1.

Fig.6 External clock.



For parameter description see Table 1.

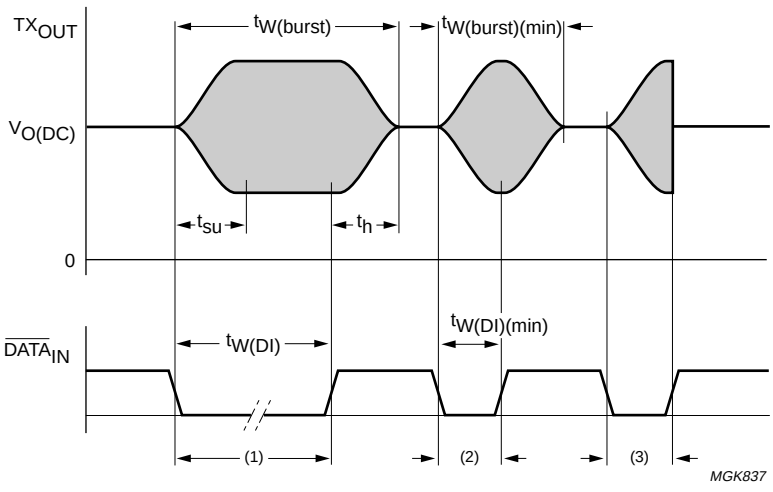
Fig.7 Typical configuration for on-chip clock circuit.

Table 1 Clock oscillator parameters

f_{osc} OSCILLATOR FREQUENCY	f_{cr} CARRIER FREQUENCY	$\frac{1}{2}f_{osc}$ CLOCK OUTPUT FREQUENCY	EXTERNAL COMPONENTS
6.080 to 9.504 MHz	95 to 148.5 kHz	3.040 to 4.752 MHz	C1 = C2 = 27 to 47 pF; R_p = 2.2 to 4.7 MΩ; XTAL = standard quartz crystal

Table 2 Calculation of parameters depending of the clock frequency

SYMBOL	PARAMETER	CONDITIONS	UNIT
f_{osc}	oscillator frequency	with on-chip oscillator: frequency of the crystal quartz; with external clock: frequency of the signal applied at OSC1	Hz
f_{CLKOUT}	clock output frequency	$\frac{1}{2}f_{osc}$	Hz
f_{cr}	carrier frequency/digital filter tuning frequency	$\frac{1}{64}f_{osc}$	Hz
t_{su}	set-up time of the shaped burst	$\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$	s
t_h	hold time of the shaped burst	$\frac{23}{f_{cr}}$ or $\frac{1472}{f_{osc}}$	s
$t_{W(DI)(min)}$	minimum pulse width of $\overline{DATA}_{IN}$ signal	$t_{su} + \frac{1}{f_{cr}}$	s
$t_{W(burst)(min)}$	minimum burst time of $V_{O(DC)}$ signal	$t_{W(DI)(min)} + t_h$	s
$t_{c(AGC)}$	AGC time constant	$\frac{2514}{f_{osc}}$	s
$t_{su(demod)}$	demodulation set-up time	$\frac{3700}{f_{osc}}$ (≈max.)	s
$t_{h(demod)}$	demodulation hold time	$\frac{3050}{f_{osc}}$ (≈max.)	s



(1) $t_{W(DI)} > t_{W(DI)(min)}$

(2) $t_{W(DI)(min)} = t_{su} + \frac{1}{f_{cr}}$

(3) $t_{W(DI)(min)} < t_{su}$; wrong operation

Fig.8 Relationship between $\overline{DATA}_{IN}$ and TX_{OUT} (see Table 3).

Table 3 Relationship between $\overline{DATA}_{IN}$ and TX_{OUT}

PD	$\overline{DATA}_{IN}$	TX_{OUT}
1	X(1)	high impedance
0	1	high impedance (after t_h)
0	0	**active** with DC offset

Note

1. X = don't care.

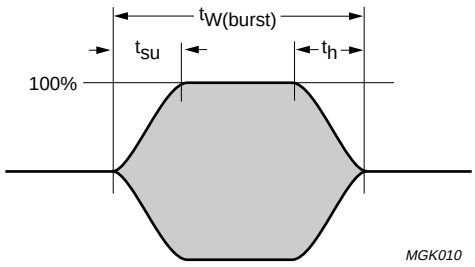
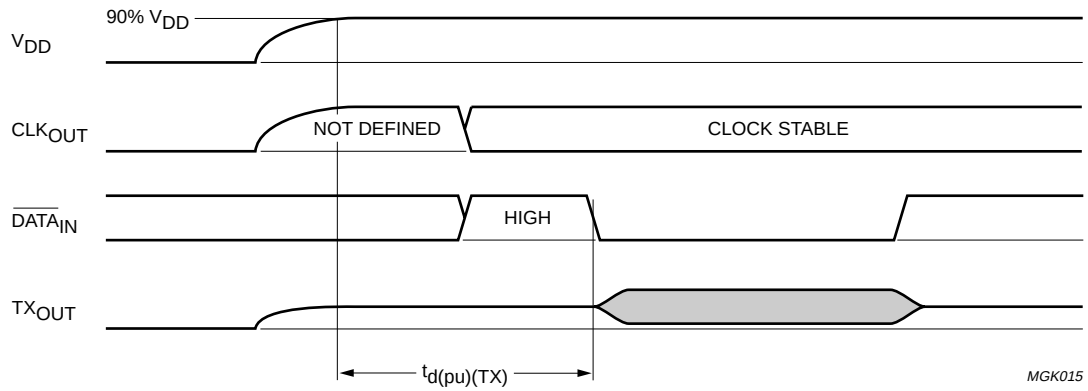


Fig.9 Pulse shape characteristics.

Timing diagrams



$\overline{DATA}_{IN}$ is an edge-sensitive input and must be HIGH before starting a transmission.

Fig.10 Timing diagram during power-up in transmission mode.

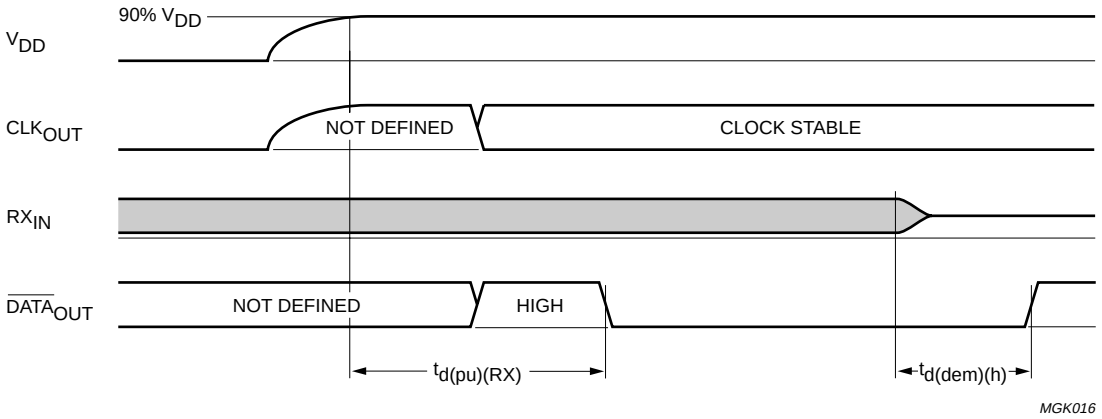


Fig.11 Timing diagram during power-up in reception mode.

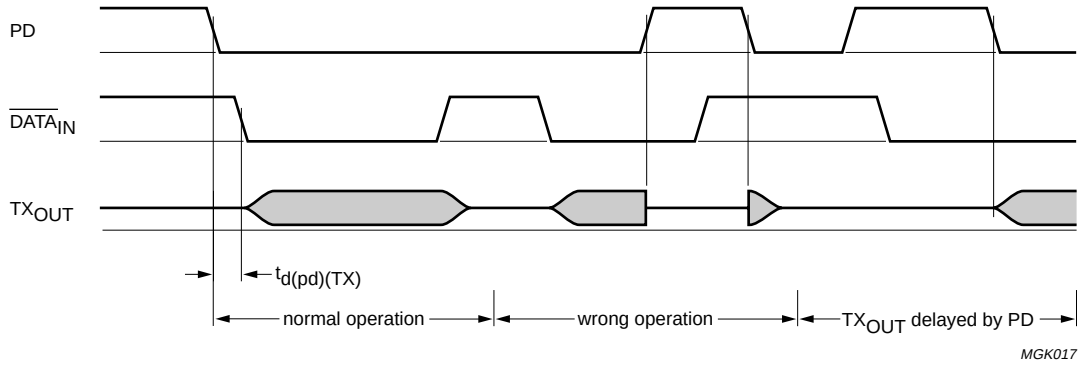


Fig.12 Power-down sequence in transmission mode.

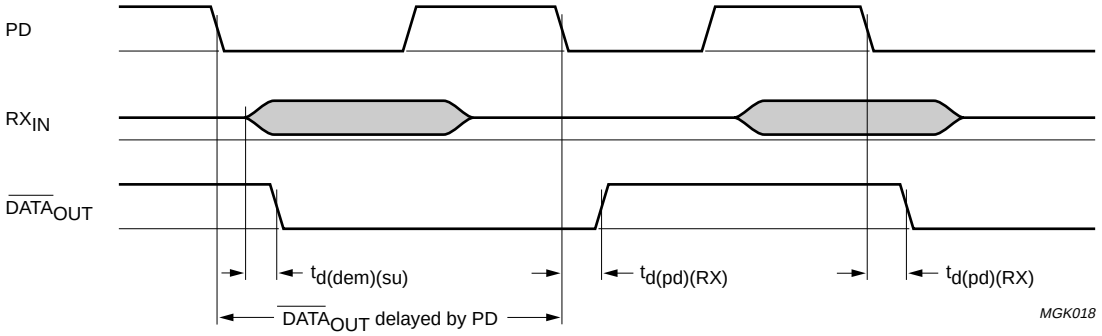


Fig.13 Power-down sequence in reception mode.

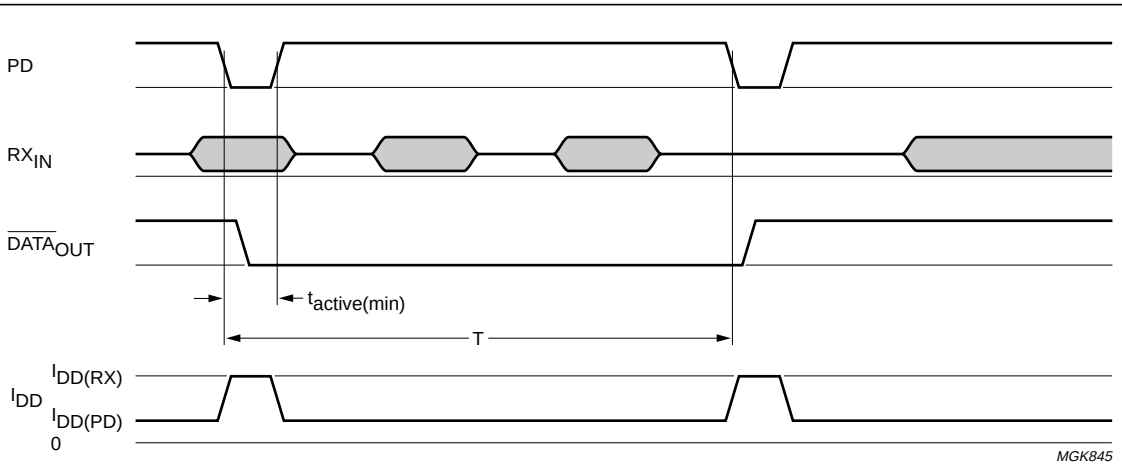


Fig.14 Power saving by dynamic control of power-down.

TEST INFORMATION

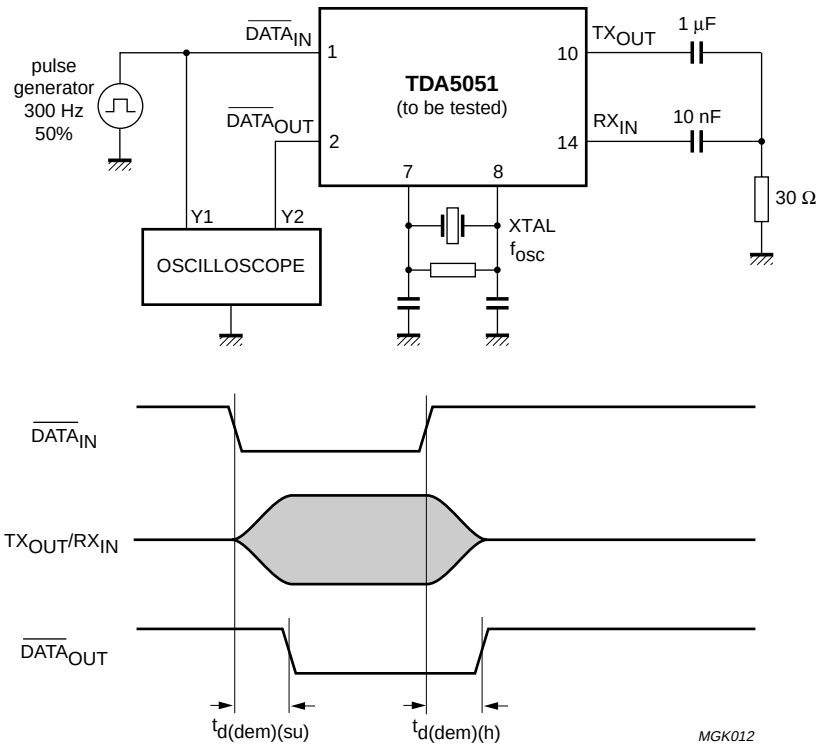
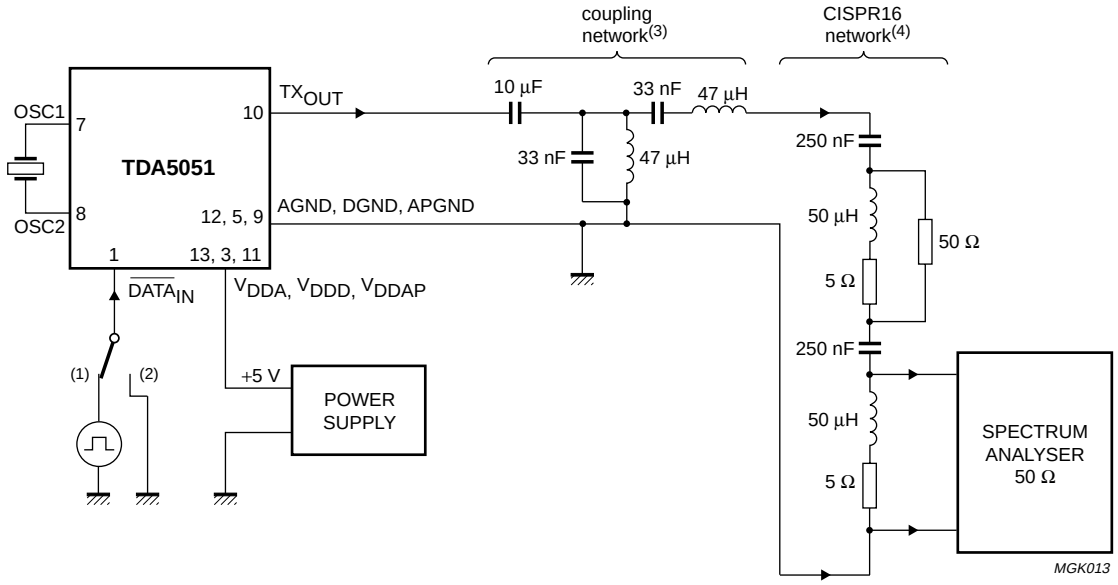


Fig.15 Test set-up for measuring demodulation delay.



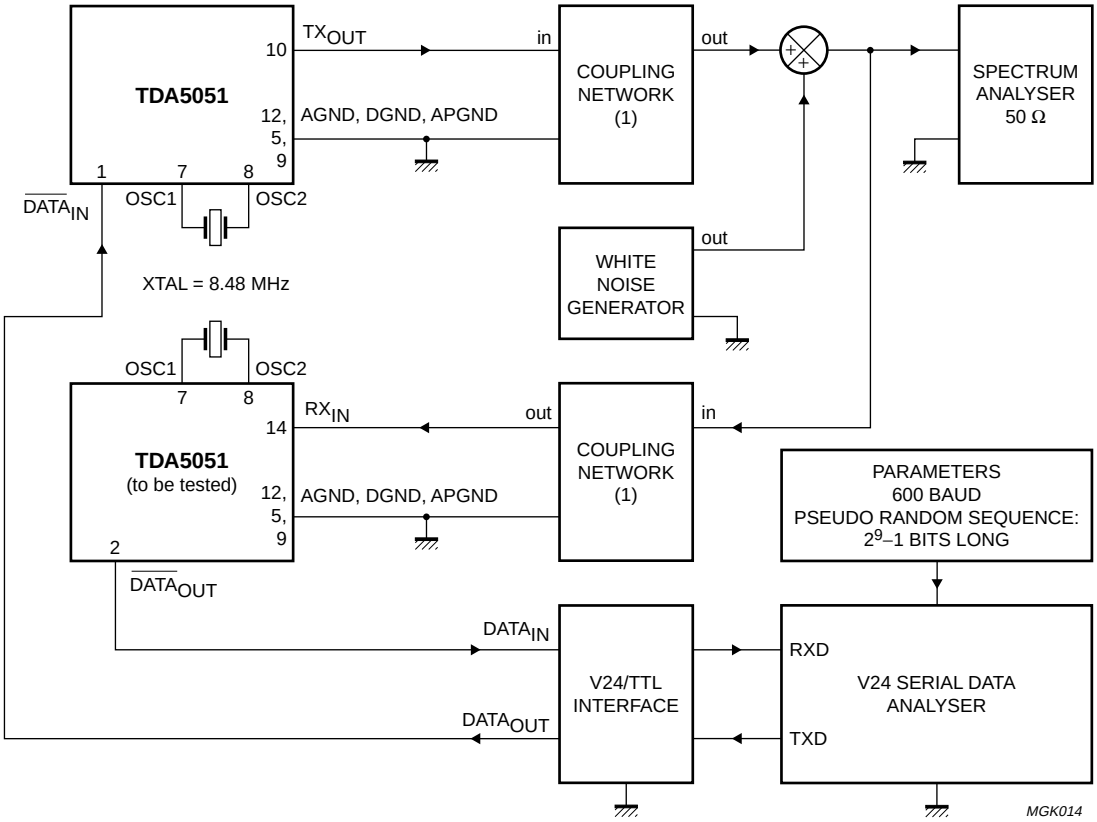
(1) Square wave TTL signal 300 Hz, duty factor = 50% for measuring signal bandwidth (see spectrum Fig.3).

(2) $\overline{DATA}_{IN}$ = LOW for measuring total harmonic distortion (see spectrum Fig.3).

(3) Tuned for f_{cr} = 132.5 kHz.

(4) The CISPR16 network provides a −6 dB attenuation.

Fig.16 Test set-up for measuring THD and bandwidth of the TX_{OUT} signal.



(1) See Fig.16.

Fig.17 Test set-up for measuring bit error rate (BER).

APPLICATION INFORMATION

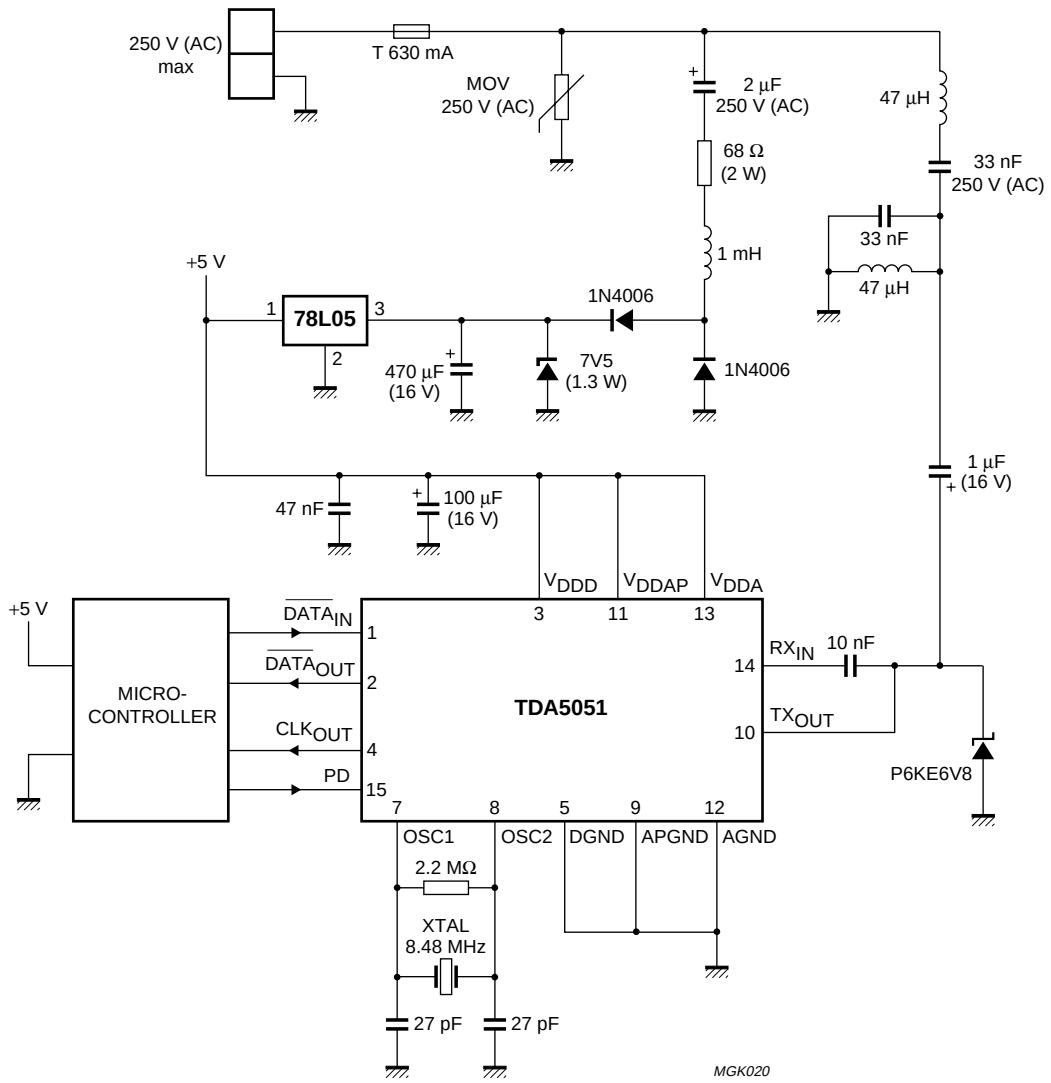
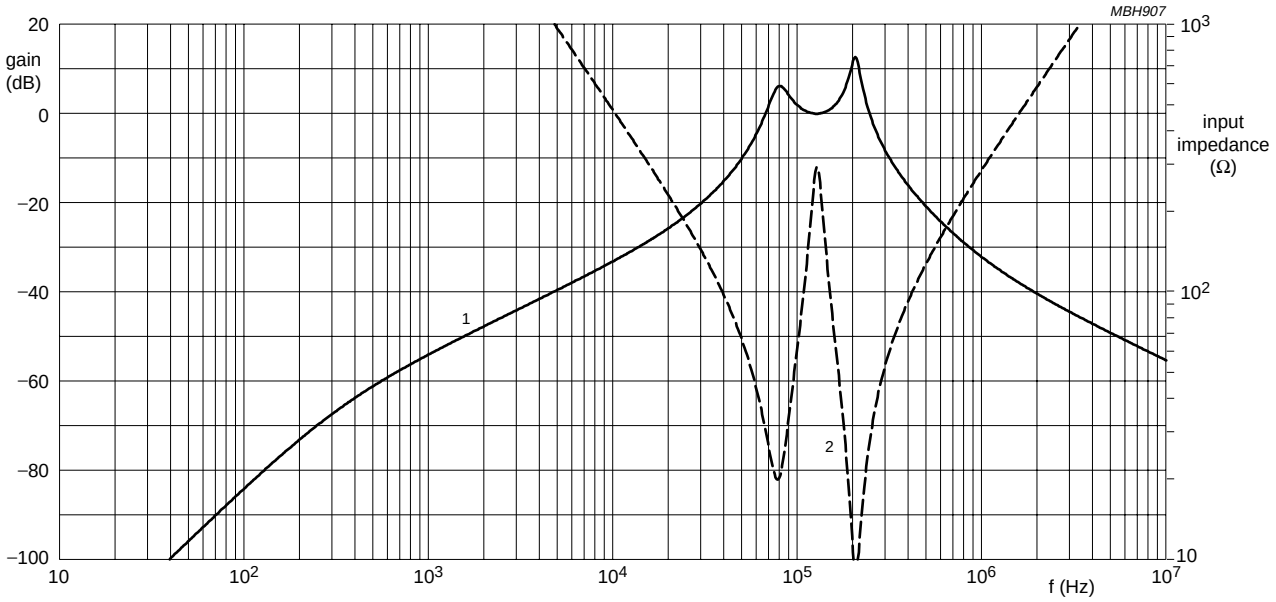
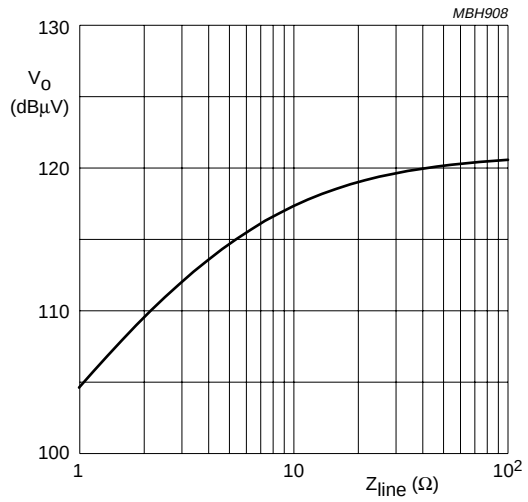


Fig.18 Application diagram without power line insulation.



Main features of the coupling network: 50 Hz rejection >80 dB; anti-aliasing for the digital filter >50 dB at the sampling frequency ($\frac{1}{2}f_{osc}$). Input impedance always higher than 10 Ω within the 95 to 148.5 kHz band.

Fig.19 Gain (curve 1) and input impedance (curve 2) of the coupling network (f_{cr} = 132.5 kHz); L = 47 μH; C = 33 nF.



Main features of the coupling network: 50 Hz rejection >80 dB; anti-aliasing for the digital filter >50 dB at the sampling frequency ($\frac{1}{2}f_{osc}$). Input impedance always higher than 10 Ω within the 95 to 148.5 kHz band.

Fig.20 Output voltage versus line impedance (with coupling network); L = 47 μH; C = 33 nF.

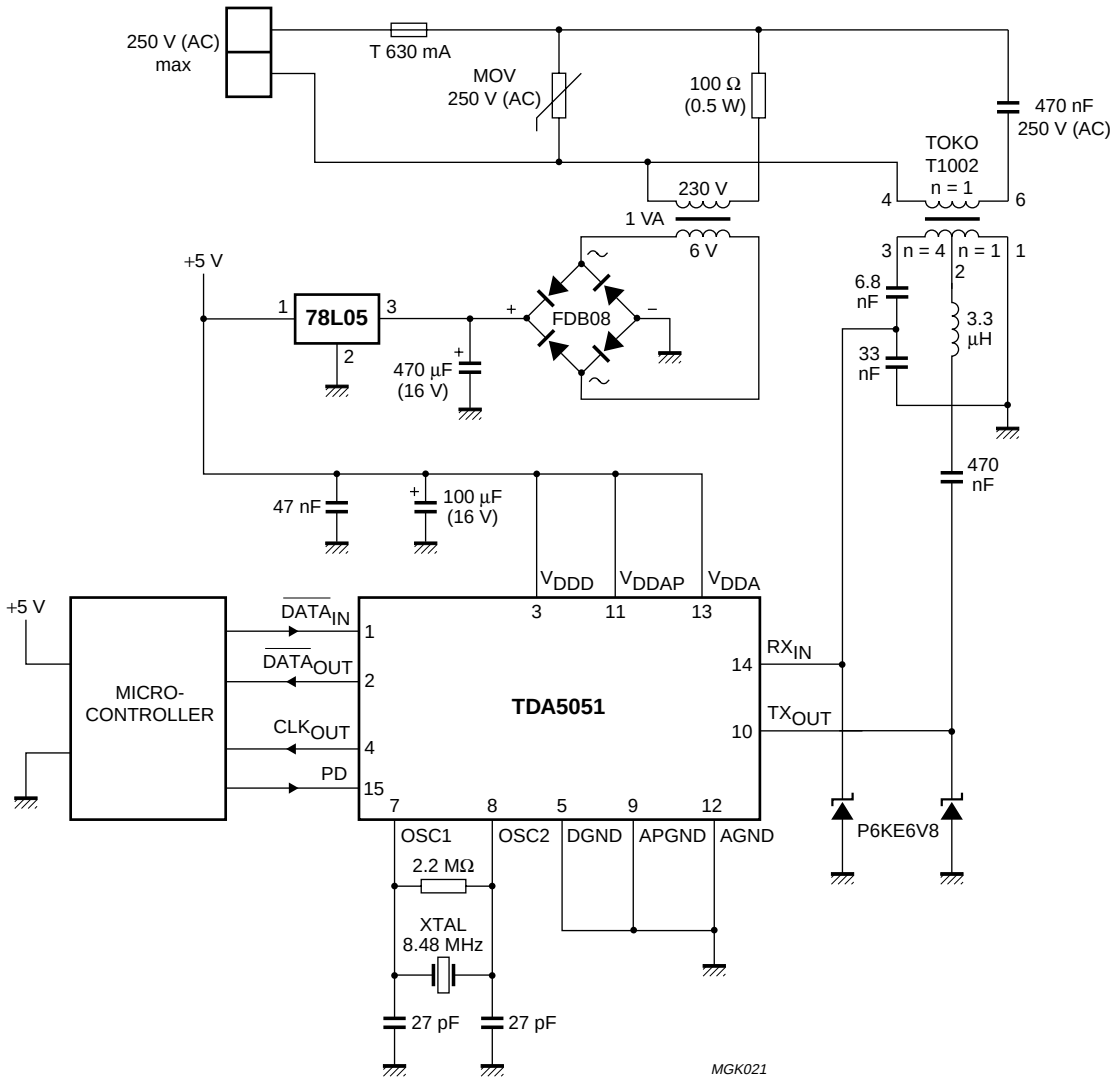
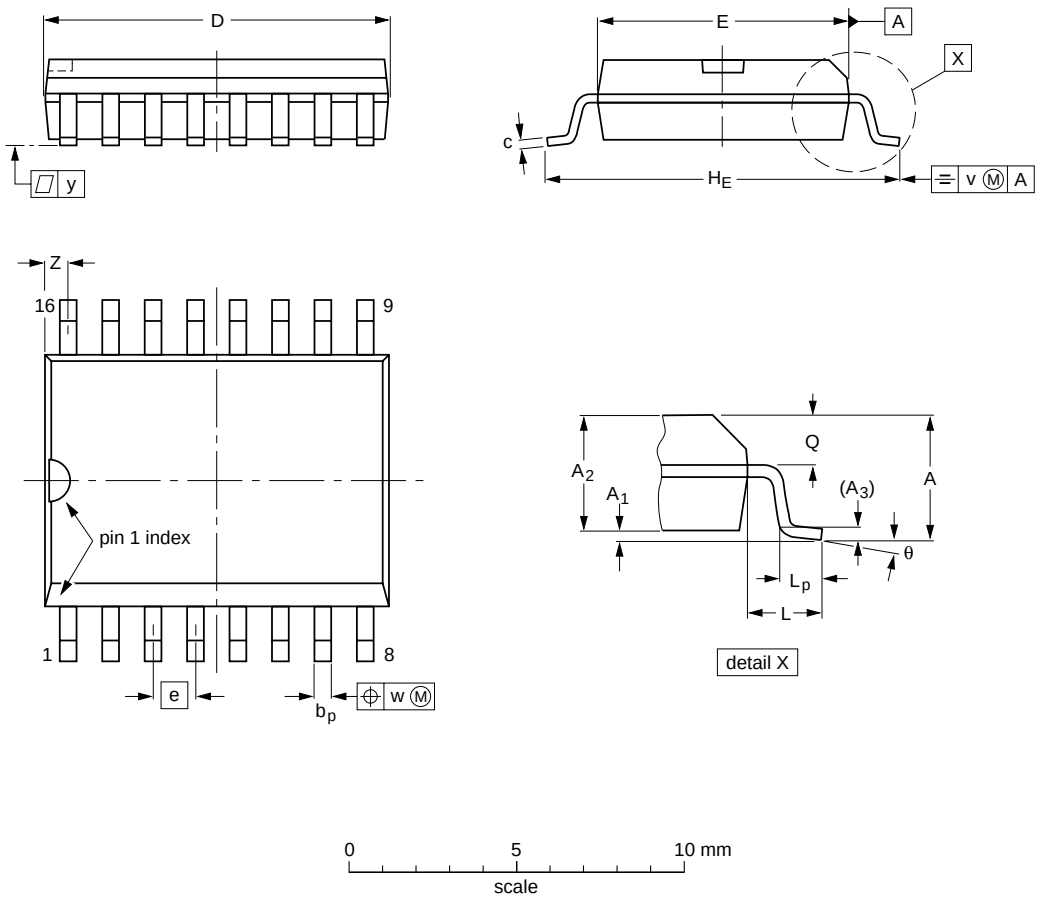


Fig.21 Application diagram with power line insulation.

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
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For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Printed in The Netherlands 297027/1200/02/pp28 Date of release: 1997 Sep 19 Document order number: 9397 750 02513

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