Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVERS

IDT54/74FCT240T/AT/CT/DT - 2240T/AT/CT
IDT54/74FCT244T/AT/CT/DT - 2244T/AT/CT
IDT54/74FCT540T/AT/CT
IDT54/74FCT541/2541T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT240T/FCT244T/FCT540T/FCT541T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
- **Features for FCT2240T/FCT2244T/FCT2541T:**
  - Std., A and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

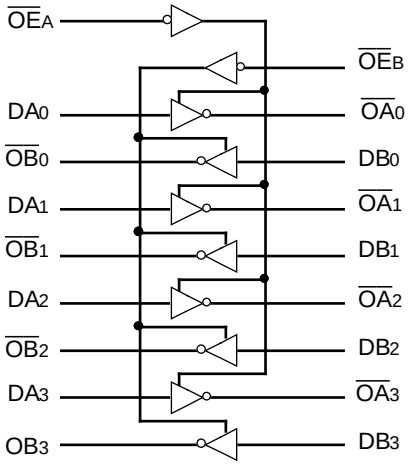
DESCRIPTION:

The IDT octal buffer/line drivers are built using an advanced dual metal CMOS technology. The FCT240T/FCT2240T and FCT244T/FCT2244T are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

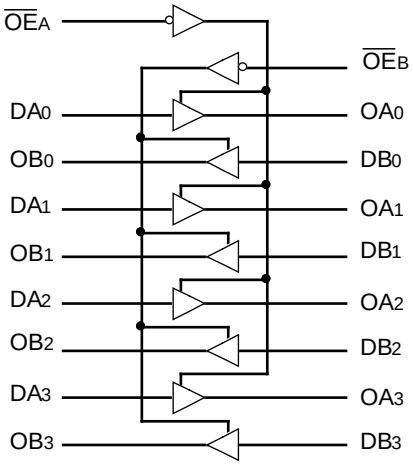
The FCT540T and FCT541T/FCT2541T are similar in function to the FCT240T/FCT2240T and FCT244T/FCT2244T, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

The FCT2240T, FCT2244T and FCT2541T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

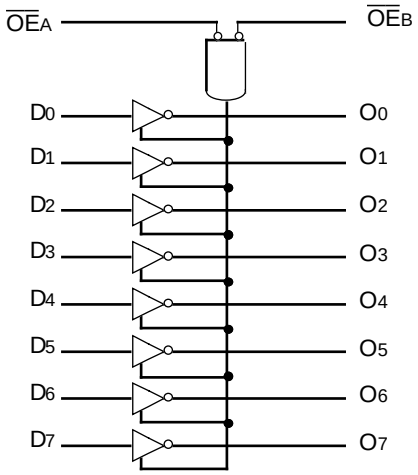
FUNCTIONAL BLOCK DIAGRAMS



FCT240/2240T



FCT244/2244T



FCT540/541/2541T

*Logic diagram shown for 'FCT540.
'FCT541/2541T is the non-inverting option.

2565 drw 01

2565 drw 02

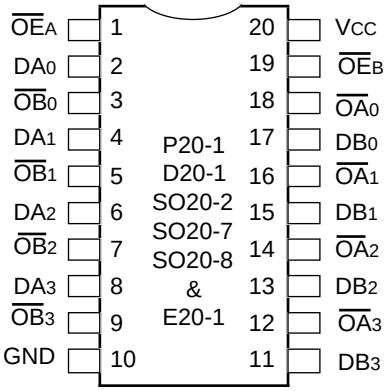
2565 drw 03

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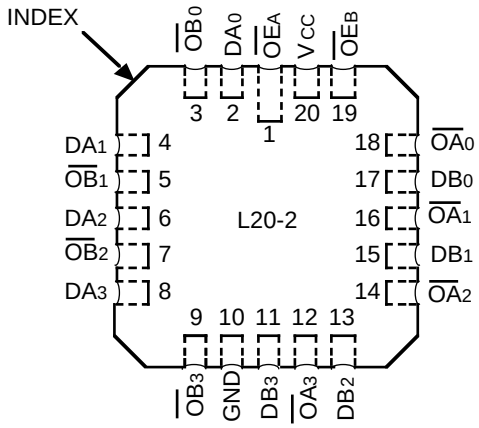
PIN CONFIGURATIONS

FCT240/2240T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

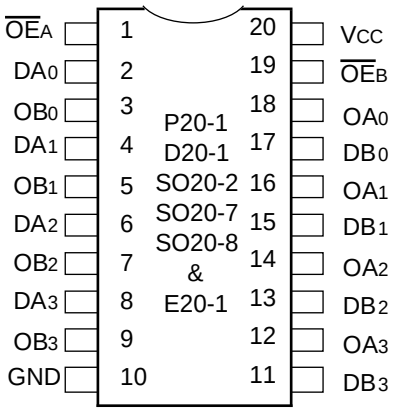
2565 drw 04



LCC
TOP VIEW

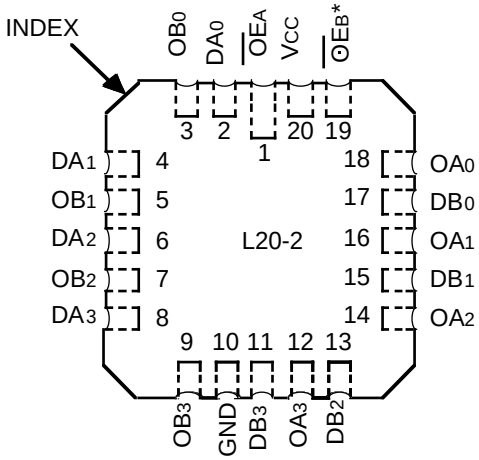
2565 drw 07

FCT244/2244T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

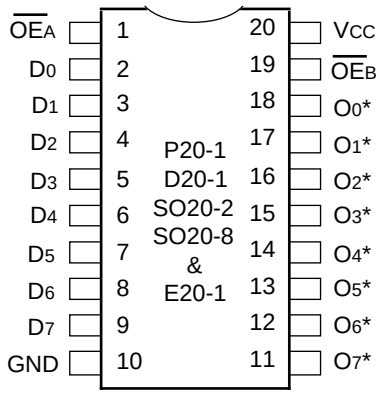
2565 drw 05



LCC
TOP VIEW

2565 drw 08

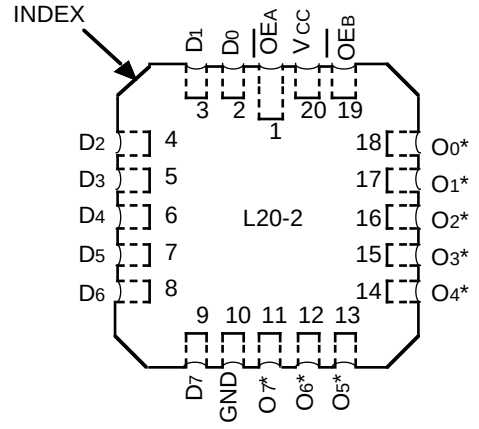
FCT540/541/2541T



DIP/SOIC/QSOP/CERPACK
TOP VIEW

*$\overline{O}$x for 540, Ox for 541/2541T

2565 drw 06



LCC
TOP VIEW

2565 drw 09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3–State Output Enable Inputs (Active LOW)
Dxx	Inputs
Oxx	Outputs

2565 tbl 01

FUNCTION TABLE

Inputs[1]			Outputs[1]			
$\overline{OE}_A$	$\overline{OE}_B$	D	240	244	540	541
L	L	L	H	L	H	L
L	L	H	L	H	L	H
H	H	X	Z	Z	Z	Z

2565 tbl 02

NOTES:
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2565 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2565 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2565 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT240/244/540/541T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA

2565 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2240/2244/2541T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2565 lnk 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
		One Input Toggling 50% Duty Cycle		FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max.	V_{IN} = V_{CC}	FCTxxxT	—	1.5	3.5	mA
		Outputs Open fi = 10MHz	V_{IN} = GND	FCT2xxxT	—	0.6	2.2	
		50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND	V_{IN} = 3.4	FCTxxxT	—	1.8	4.5	
		One Bit Toggling	V_{IN} = GND	FCT2xxxT		0.9	3.2	
		V_{CC} = Max.	V_{IN} = V_{CC}	FCTxxxT	—	3.0	6.0[5]	
		Outputs Open fi = 2.5MHz	V_{IN} = GND	FCT2xxxT	—	1.2	3.4[5]	
		50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND	V_{IN} = 3.4	FCTxxxT	—	5.0	14.0[5]	
		Eight Bits Toggling	V_{IN} = GND	FCT2xxxT	—	3.2	11.4[5]	

2565 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240/2240T

			FCT240T FCT2240T				FCT240AT FCT2240AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns

2565 tbl 09

			FCT240CT FCT2240CT				FCT240DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	4.7	1.5	3.6	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT244/2244T

			FCT244T FCT2244T				FCT244AT FCT2244AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2565 tbl 11

			FCT244CT FCT2244CT				FCT244DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	4.1	1.5	4.6	1.5	3.6	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 12

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540/541/2541T

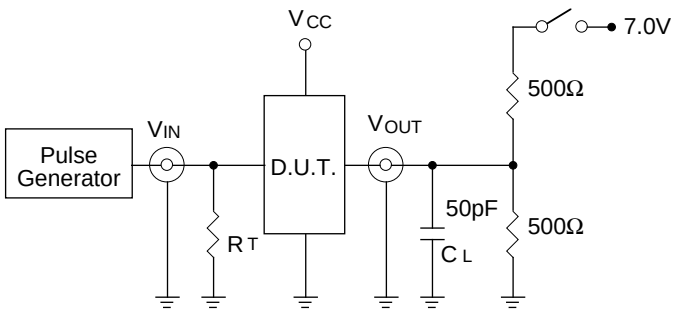
Symbol	Parameter	Condition[1]	FCT540T/541T FCT2541T				FCT540AT/541AT FCT2541AT				FCT540CT/541CT FCT2541CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$ FCT540	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N FCT541/2541T		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2565 tbl 13

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2565 drw 10

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

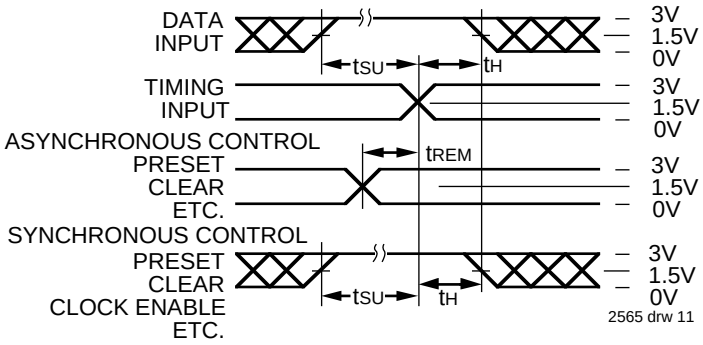
2565 drw 14

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

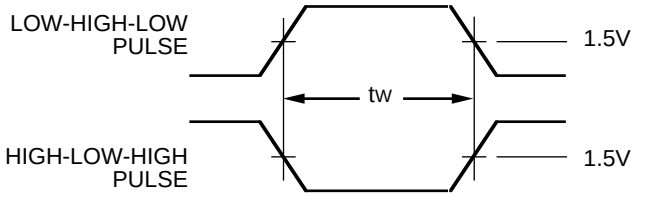
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



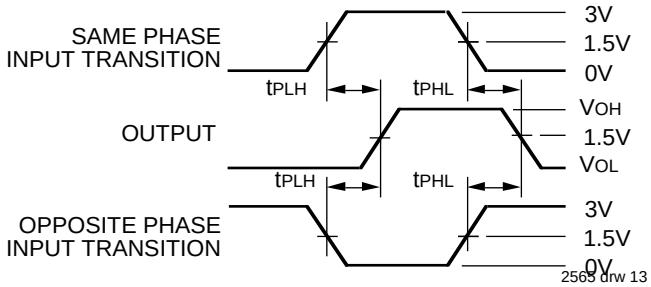
2565 drw 11

PULSE WIDTH



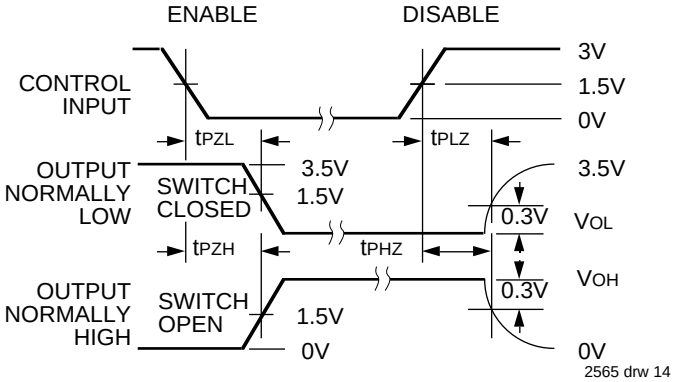
2565 drw 12

PROPAGATION DELAY



2565 drw 13

ENABLE AND DISABLE TIMES

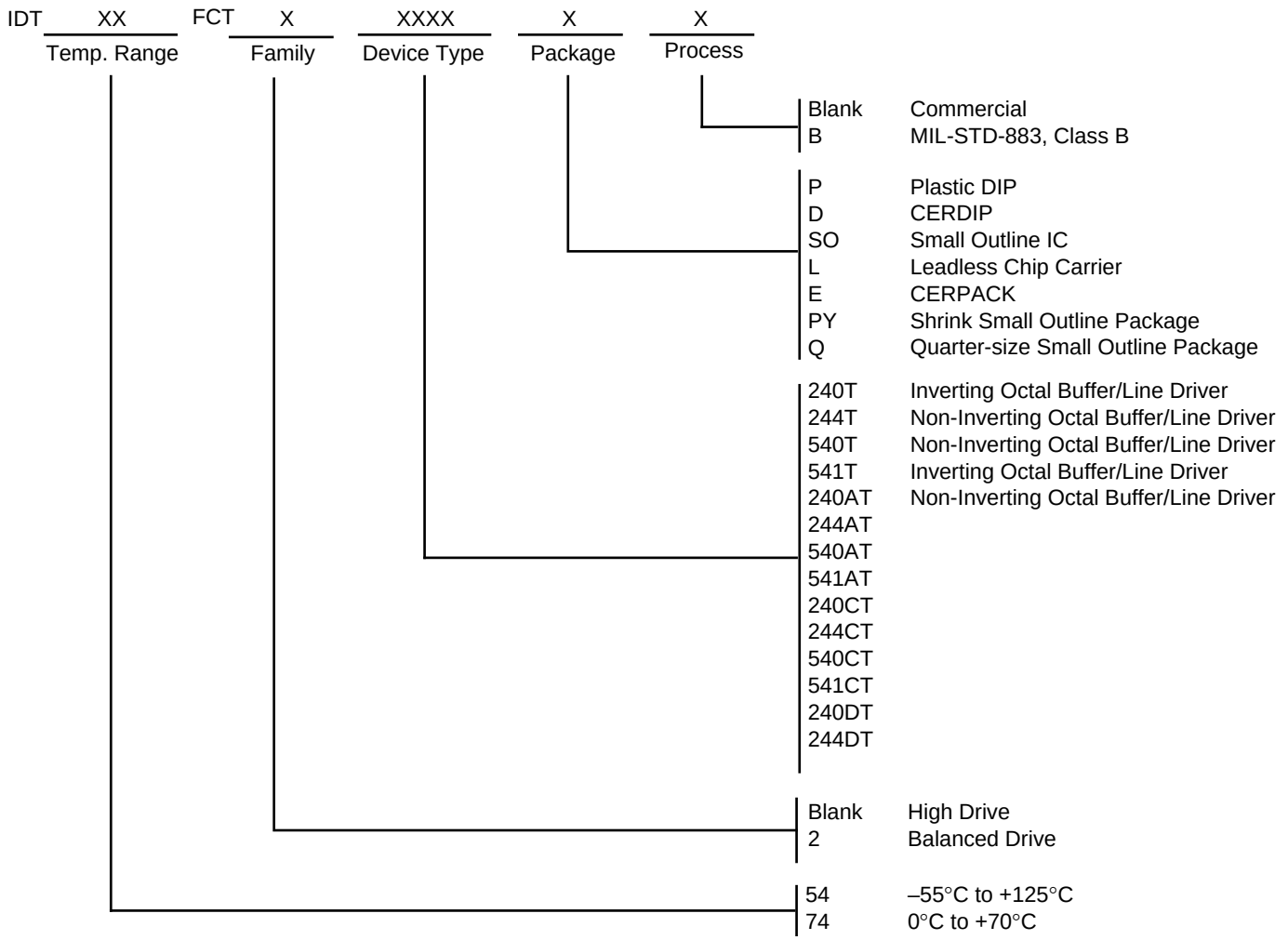


2565 drw 14

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2565 drw 15