To all our customers

# Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Not recommend for new design

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

# M62399P,FP

## 8-BIT 8CH I²C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

## DESCRIPTION

The M62399P,FP is an integrated circuit semiconductor of high voltage type CMOS structure with 8 channels of built-in D-A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer formal of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 2.5mA or more,and it operates in the whole voltage range from VrefU to ground.

And because of connects maximum 8 pieces,it is possible to 64 channels control.

## FEATURES

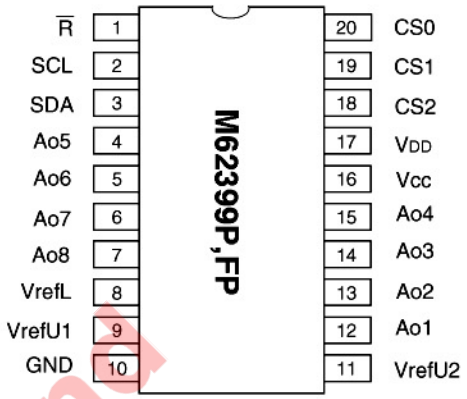
- Digital data transfer format
  I²C-bus serial data method
- Output buffer operational amplifier
  it operates in the whole voltage range from VrefU(0~12V)to ground.
- High output current drive capacity
  ±2.5mA over
- Preparation two high level reference voltage terminal
  because there are two high level reference voltage terminal,it can set up two kinds differ voltage range.

## APPLICATION

Conversion from digital control data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of DISPLAY-MONITOR or CTV.

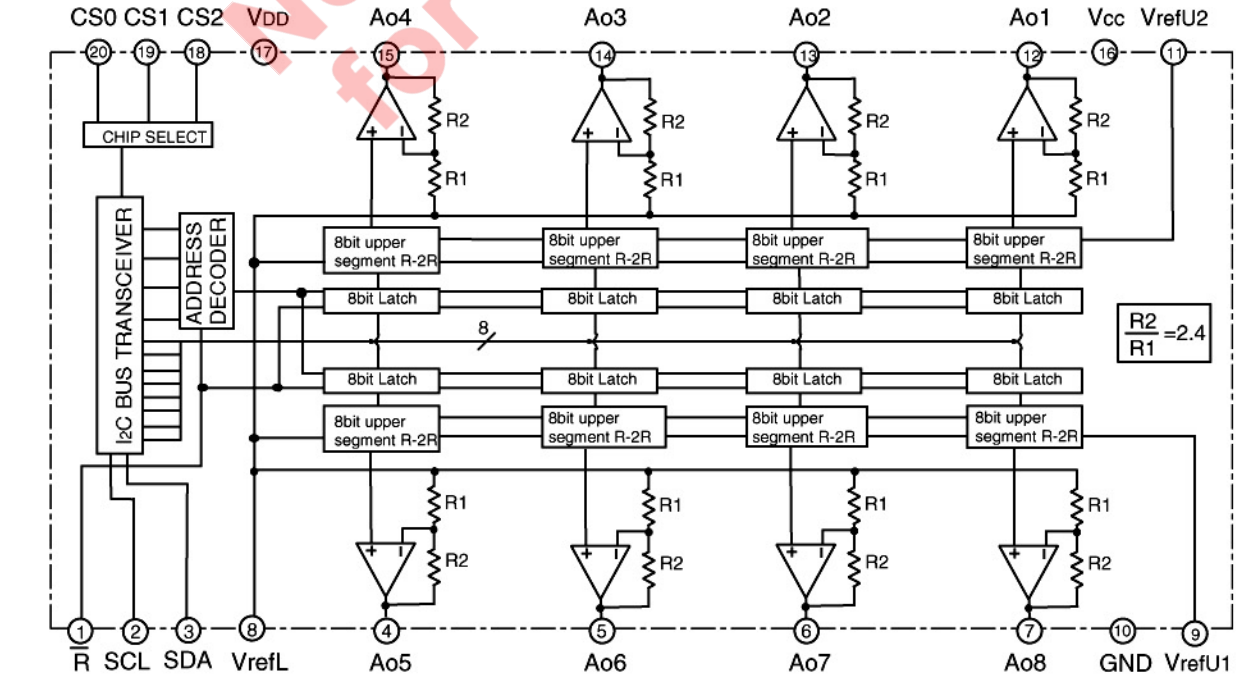
## PIN CONFIGURATION (TOP VIEW)




Outline 20P4(P)
20P2N-A(FP)

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## BLOCK DIAGRAM



## EXPLANATION OF TERMINALS

| Pin No. | Symbol | Function |
|---|---|---|
| ③ | SDA | Serial data input terminal |
| ① | $\overline{R}$ | Reset signal input terminal |
| ② | SCL | Serial clock input terminal |
| ⑫ | Ao1 | 8-bit D-A converter output terminal |
| ⑬ | Ao2 | |
| ⑭ | Ao3 | |
| ⑮ | Ao4 | |
| ④ | Ao5 | |
| ⑤ | Ao6 | |
| ⑥ | Ao7 | |
| ⑦ | Ao8 | |
| ⑯ | $V_{CC}$ | Analog power supply terminal |
| ⑰ | $V_{DD}$ | Digital power supply terminal |
| ⑩ | GND | Analog and digital common GND |
| ⑧ | VrefL | D-A converter low level reference voltage input terminal |
| ⑨ | VrefU1 | D-A converter high level reference voltage input terminal 1 |
| ⑪ | VrefU2 | D-A converter high level reference voltage input terminal 2 |
| ⑱ | CS2 | Chip select data input terminal 2 |
| ⑲ | CS1 | Chip select data input terminal 1 |
| ⑳ | CS0 | Chip select data input terminal 0 |

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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | -0.3~+13.5 | V |
| $V_{DD}$ | Supply voltage | | -0.3~+7.0 | V |
| VrefU1,2 | D-A converter upper reference voltage | | $V_{DD}$ | V |
| $V_{IND}$ | Digital input voltage | | -0.3~$V_{DD}$+0.3 | V |
| Topr | Operating temperature | | -20~+85 | °C |
| Tstg | Storage temperature | | -40~+125 | °C |

## ELECTRICAL CHARACTERISTICS

**Digital part**(Vcc=13V,$V_{DD}$=VrefU1,2=+5V±10%,GND=VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $I_{DD}$ | Supply current | CLK=1MHz operation $I_{AO}$=0μA | | | 1 | mA |
| $I_{ILK}$ | Input leak current | $V_{IN}$=0~$V_{DD}$ | -10 | | 10 | μA |
| $V_{IL}$ | Input low voltage | | | | 0.2$V_{CC}$ | V |
| $V_{IH}$ | Input high voltage | | 0.8$V_{CC}$ | | | V |

**Analog part**(Vcc=13V,$V_{DD}$=VrefU1,2=+5V±10%,GND=VrefL=0V,Ta=-20 ~ +85°C,unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vcc | Supply voltage | | $V_{DD}$ | | 13 | V |
| Icc | Circuit current | CLK=1MHz operation $I_{AO}$=0μA | | 2.0 | 4.0 | mA |
| IrefU | D-A converter upper reference voltage input current | VrefU=5V VrefL=0V<br>Data condition:at maximum current | | 1.2 | 2.5 | mA |
| VrefU | D-A converter upper reference voltage range | The output does not necessarily be the values within the reference voltage setting range. | 3.5 | | $V_{DD}$ | V |
| VrefL | D-A converter lower reference voltage range | | GND | | 1.5 | V |
| $V_{AO}$ | Buffer amplifier output voltage range | $I_{AO}$=±500μA | 0.1 | | Vcc-0.1 | V |
| | | $I_{AO}$=±1.0mA | 0.2 | | Vcc-0.2 | |
| $I_{AO}$ | Buffer amplifier output drive range | Upper side saturation voltage=0.3V<br>Lower side saturation voltage=0.2V | -2.5 | | 2.5 | mA |
| $S_{DL}$ | Differential nonlinearity error | VrefU=4.79V<br>VrefL=0.95V<br>Vcc=5.5V(15mV/LSB)<br>without load($I_{AO}$=0) | -1.0 | | 1.0 | LSB |
| $S_L$ | Nonlinearity error | | -1.5 | | 1.5 | LSB |
| $S_{ZERO}$ | Zero code error | | -2.0 | | 2.0 | LSB |
| $S_{FULL}$ | Full scale error | | -2.0 | | 2.0 | LSB |
| Eo | Gain error | | -3.0 | | 3.0 | % |
| SR | Output slew rate | | | 0.2 | | V/μs |

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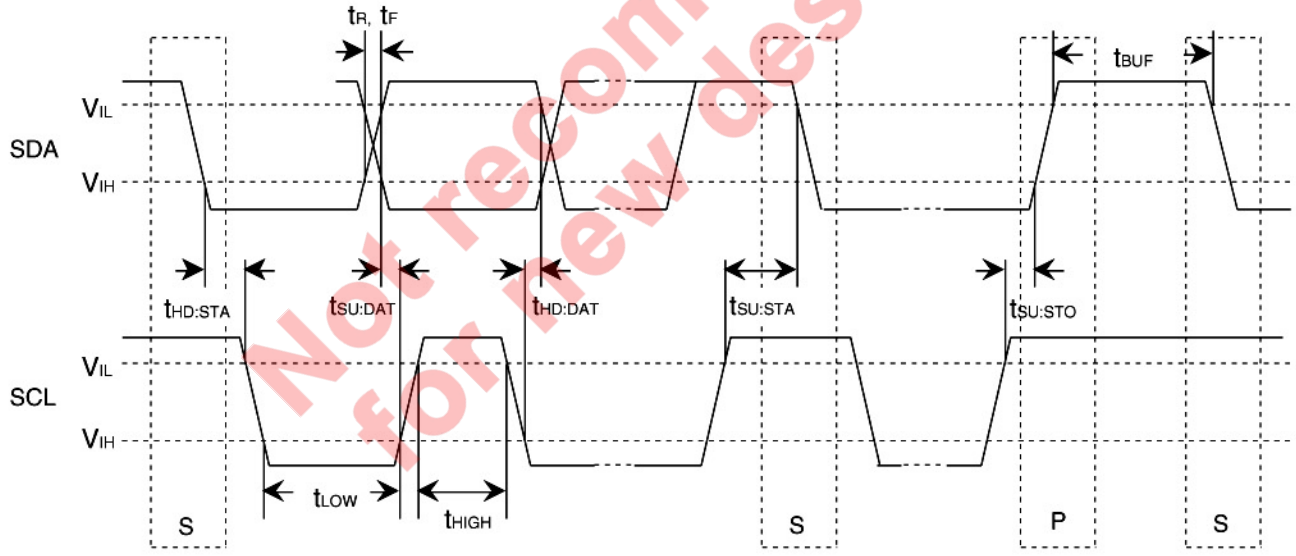
## I²C-BUS LINE CHARACTERISTICS

| Symbol | Parameter | Normal mode | | High speed mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | KHz |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 4.7 | — | 1.3 | — | μs |
| $t_{HD:STA}$ | Hold time start condition.After this period.The first clock pulse is generated | 4.0 | — | 0.6 | — | μs |
| $t_{LOW}$ | The low period of the clock | 4.7 | — | 1.3 | — | μs |
| $t_{HIGH}$ | The high period of the clock | 4.0 | — | 0.6 | — | μs |
| $t_{SU:STA}$ | Set up time for start condition(only relevant for a repeated start condition) | 4.7 | — | 4.7 | — | μs |
| $t_{HD:DAT}$ | Hold time data | 0 | — | 0 | 0.9 | μs |
| $t_{SU:DAT}$ | Set up time data | 250 | — | 100 | — | ns |
| $t_R$ | Rise time of both SDA and SCL lines | — | 1000 | 20 | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL lines | — | 300 | 20 | 300 | ns |
| $t_{SU:STO}$ | Set up time for stop condition | 4.0 | — | 0.6 | — | μs |

*Note that transmitter must internally at reset a hold time to bridge the undefined region(max.300ns)of the falling edge of SCL.

Not recommend for new design

## TIMING CHART



## I2C BUS FORMAT

| STA | SLAVE ADDRESS | W | A | SUB ADDRESS | A | DAC DATA | A | STP |
|---|---|---|---|---|---|---|---|---|

## DIGITAL DATA FORMAT

•SLAVE ADDRESS

FIRST → LAST

| 1 | 0 | 0 | 1 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|

(SLAVE ADDRESS) CHIP SELECT DATA

•SUB ADDRESS

FIRST → LAST

| X | X | X | X | S3 | S2 | S1 | S0 |
|---|---|---|---|---|---|---|---|

Don't care — CHANNEL SELECT DATA

•DAC DATA

FIRST MSB → LAST LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

(1)CHIP SELECT DATA

MSB LSB

| A2 | A1 | A0 | CS2 | CS1 | CS0 |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 |

(2)CHANNEL SELECT DATA

MSB LSB

| S3 | S2 | S1 | S0 | Channel selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Don't care. |
| 0 | 0 | 0 | 1 | ch1 selection |
| 0 | 0 | 1 | 0 | ch2 selection |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 0 | 1 | 1 | 1 | ch7 selection |
| 1 | 0 | 0 | 0 | ch8 selection |
| 1 | 0 | 0 | 1 | Don't care. |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | Don't care. |

(3)DAC DATA

FIRST MSB → LAST LSB

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | DAC output |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (VrefU-VrefL)/256 x 1 x 2.4 + VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (VrefU-VrefL)/256 x 2 x 2.4 +VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | (VrefU-VrefL)/256 x 3 x 2.4 +VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | (VrefU-VrefL)/256 x 4 x 2.4 +VrefL |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | (VrefU-VrefL)/256 x 255 x 2.4 +VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | VrefU x 2.4 + VrefL |

Not recommend for new design