Audio Accessory ICs

Karaoke/Surround Digital Echo

BU9253AS/FS, BU9262AFS

●**Description**

The Karaoke/Surround Digital Echo IC incorporates a digital delay circuit, an input/output mixing circuit, supporting Karaoke echo and surround system, all in a single chip.

BU9253AS/FS has functions required by Karaoke echo system, and BU9262AFS has various functions required for surround / echo system.

●**Features**

＜BU9253AS/FS＞

1) Digital delay time : 131ms (f_{CLK} = 375kHz)
2) Built-in mixing circuit for adding original sound and echo sound
3) Echo mix ratio settable by DC voltage
4) Built-in amplifier circuit for structuring input/output secondary LPF
5) Microphone mute function (mute of mixing sound of original sound + echo sound)
6) Built-in CR oscillation circuit

＜BU9262AFS＞

1) Digital delay time : 8-stage setting from 9.2ms to 192ms
2) Built-in input/output mixing circuit
3) Built-in feedback, delay volume circuit
4) Built-in input/output LPF
5) Serial interface
6) Auto mute circuit built in (action at power on, mode switching)
7) Built-in auto reset circuit at power on

●**Applications**

Radio cassette recorder, mini-component and karaoke systems.

●**Product lineup**

Parameter	BU9253AS	BU9253FS	BU9262AFS
Supply voltage	4.0V～5.5V	4.0V～5.5V	4.5V～5.5V
Oscillation frequency	375kHz	375kHz	2MHz
Current consumption	6mA	6mA	20mA
Operating temperature range	-10～+70℃	-10～+70℃	-10～+70℃
Package	SDIP18	SSOP-A16	SSOP-A32
Digital delay	Fixed	Fixed	Variable
Echo level	Fixed	Fixed	Variable

Ver.B Oct.2005

●Absolute maximum ratings

＜BU9253AS＞

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CCMAX}	7.0	V
Terminal voltage	V_{IN}	-0.3 ～ V_{CC}+0.3	V
Power dissipation	P_D	600*	mW
Storage temperature	T_{STG}	-55 ～ +125	℃

* Reduce by 6.0 mW/°C over 25°C

＜BU9253FS＞

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CCMAX}	7.0	V
Terminal voltage	V_{IN}	-0.3 ～ V_{CC}+0.3	V
Power dissipation	P_D	500*	mW
Storage temperature	T_{STG}	-55 ～ +125	℃

* Reduce by 5.0 mW/°C over 25°C

＜BU9262AFS＞

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	0.3 ～ 7.0	V
Terminal voltage	V_{IN}	V_{SS} – 0.3 ～ V_{CC} + 0.3	V
Power dissipation	P_D	800*	mW
Storage temperature	T_{STG}	-55 ～ +125	℃

* Reduce by 8.0 mW/°C over 25°C

Note: This IC is not designed to be radiation-resistant.
Note: Operation is not guaranteed.

●Operating conditions

＜BU9253AS/FS＞

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	4.0 ～ 5.5	V
Operating temperature	Ta	-10 ～ +70	℃
Operating frequency	f_C	375	kHz

＜BU9262AFS＞

Parameter	Symbol	Limits	Unit
Operating supply range	V_{CC}	4.5 ～ 5.5	V
Operating temperature	Ta	-10 ～ +70	℃
Operating frequency	f_C	2	MHz

●Electrical characteristics

＜BU9253AS/FS＞

(Ta=25℃, V_{CC}=5.0V, f_C=375kHz, f_{in}=1kHz, V_I=-10dBV, ECHO VR pin=V_{CC}, MUTE pin=V_{CC}, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Circuit Current	I_{CC}	–	6	12	mA	No signal input
Voltage Gain 1	G_{V1}	-5.6	-3.5	-1.4	dB	Delay side total gain IN→OUT
Voltage Gain 2	G_{V2}	-1	0	-1	dB	Through side total gain IN→OUT、ECHO VR pin=GND
Output distortion 1	THD1	–	1.5	3	%	Delay side
Output distortion 2	THD2	–	0.02	0.1	%	Through side ECHO VR pin=GND
Output noise voltage 1	V_{NO1}	–	-80	-60	dBV	Delay side Rg=1kΩ
Output noise voltage 2	V_{NO2}	–	-90	-80	dBV	Through side Rg=1kΩ、ECHO VR pin=GND
Maximum output voltage 1	V_{OM1}	1.4	1.7	–	Vrms	Delay side THD=10%
Maximum output voltage 2	V_{OM2}	1.4	1.7	–	Vrms	Through side THD=1%、ECHO VR pin=GND
MUTE control voltage	V_H	3.8	–	5.0	V	H mode hold voltage MUTE pin DC
	V_M	1.6	–	2.8	V	M mode hold voltage MUTE pin DC
	V_L	0	–	0.7	V	L mode hold voltage MUTE pin DC
Oscillation frequency	f_C	–	375	–	kHz	

＜BU9262AFS＞

(Ta = 25℃, V_{CC} = 5V, V_{IN} = 200mVrms, f_{in} = 1kHz, f_C = 2MHz, Rg = 600Ω, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit current	ICC	–	20	40	mA	No signal input
[Digital delay]						
Input/Output Gain	AV1	-3	0	3	dB	
Output distortion	THD1	–	0.6	1.2	%	tDL = ～48ms、30kHz LPF
	THD2	–	1.0	2.0	%	tDL = 96ms、30kHz LPF
	THD3	–	1.2	2.4	%	tDL = 144ms、30kHz LPF
	THD4	–	1.5	3.0	%	tDL = 192ms、30kHz LPF
Output noise voltage	VNO1	–	-90	-75	dBV	tDL = ～48ms、DIN－AUDIO
	VNO2	–	-87	-72	dBV	tDL = 96ms、DIN－AUDIO
	VNO3	–	-85	-70	dBV	tDL = 144ms、DIN－AUDIO
	VNO4	–	-83	-68	dBV	tDL = 192ms、DIN－AUDIO
Maximum output voltage	VMX1	0.7	1.0	–	Vrms	THD = 10%、30kHz LPF
[Delay volume “DSIG output”]						
Input//Output Gain	AV5	0	3	6	dB	DLYVOL = MAX.
Output distortion	THD5	–	0.17	0.34	%	30kHz LPF
Output noise voltage	VNO5	–	-100	-90	dBV	DELAY OFF、DIN－AUDIO
Maximum output voltage	VMX5	1.1	1.4	–	Vrms	THD = 10%、30kHz LPF
Maximum attenuation	ATT5	–	-90	-60	dB	DLYVOL = MIN. DIN－AUDIO
[Feedback volume]						
Input/Output Gain	AV6	-6	-3	0	dB	FBVOL = MAX.
Maximum attenuation	ATT6	–	-90	-60	dB	FBVOL = MIN. DIN－AUDIO
[Line amplifier]						
Input/Output Gain	AV7	-3	0	3	dB	
Output distortion	THD6	–	0.01	0.03	%	30kHz LPF
Output noise voltage	VNO6	–	-100	-90	dBV	DELAY OFF、DIN－AUDIO
Maximum output voltage	VMX6	1.2	1.8	–	Vrms	THD = 10%、30kHz LPF
Channel separation	AVCS	–	-90	-65	dB	f = 400Hz、DIN－AUDIO
Input impedance	ZI	24	35	–	kΩ	
[Digital unit]						
Input“H”voltage	VIH	3.8	–	–	V	
Input“L”voltage	VIL	–	–	1.2	V	
Pull-up resistance	Rd	12	25	50	kΩ	
[Serial data]						
Clock width	twCK	2.0	–	–	us	
Latch width	twLT	2.0	–	–	us	
Data setup	tdsu	1.0	–	–	us	
Data hold	th	1.0	–	–	us	
Latch setup	tlsu	1.0	–	–	us	

●Reference data

＜BU9253AS/FS＞

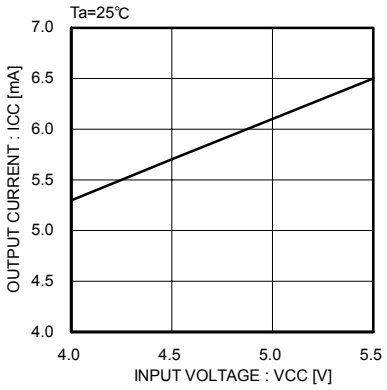


Fig.1 Current consumption

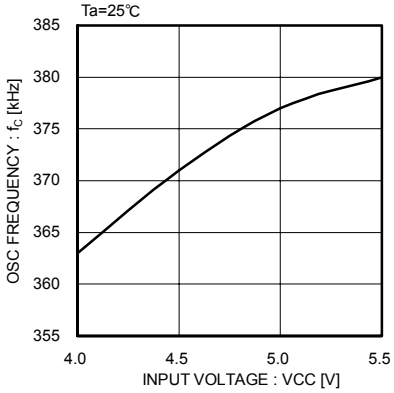


Fig.2 Oscillation frequency

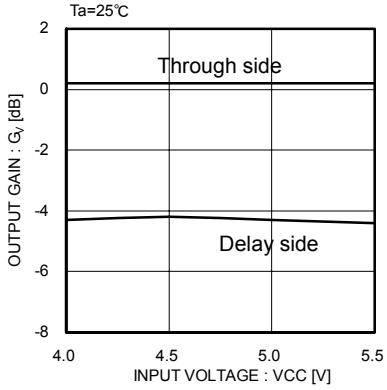


Fig.3 Total gain characteristic

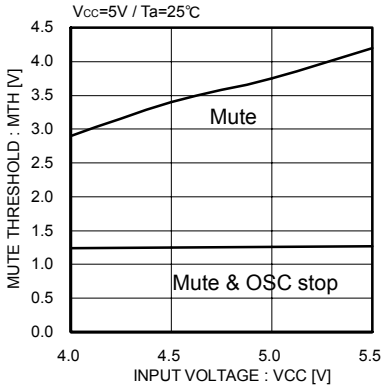


Fig.4 Mute pin threshold

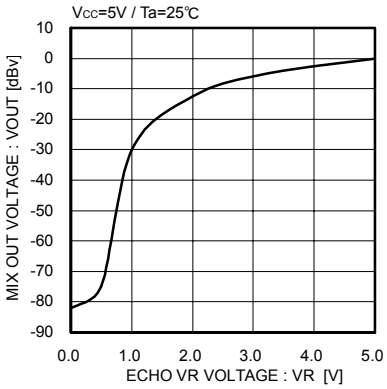


Fig.5 ECHO VR characteristic

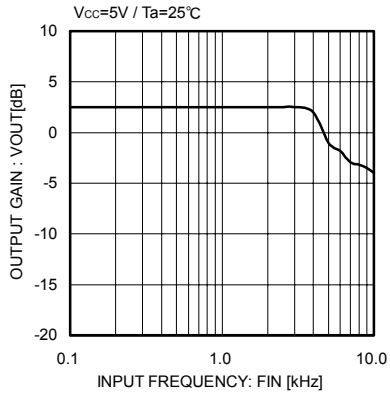


Fig.6 A/D frequency characteristic

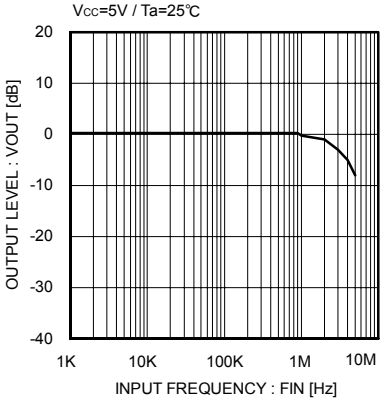


Fig.7 LPF operation amplifier frequency characteristic

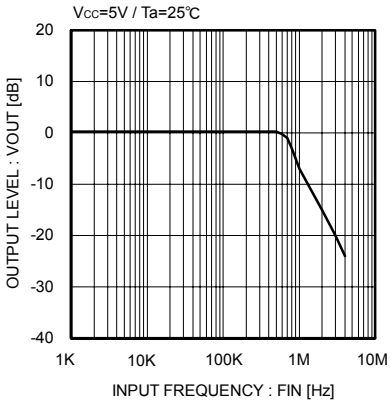


Fig.8 MIX operation amplifier frequency characteristic

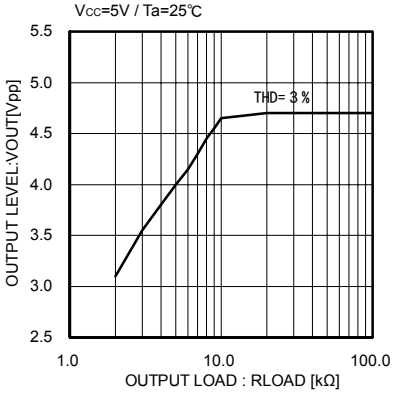


Fig.9 Through side output load drive characteristic

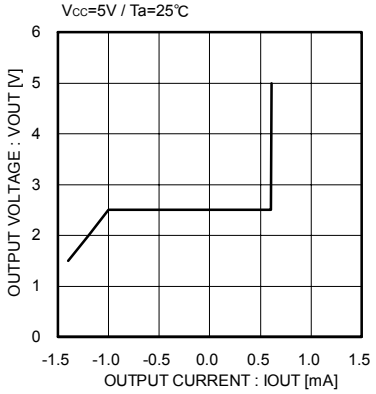


Fig.10 LPF operation amplifier output performance

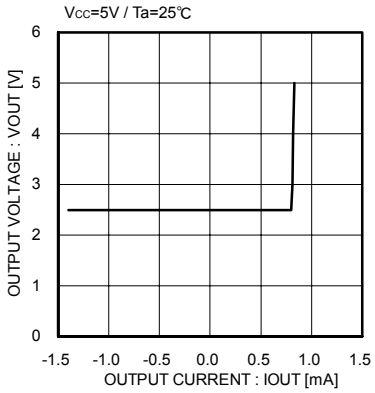


Fig.11 MIX operation amplifier output performance

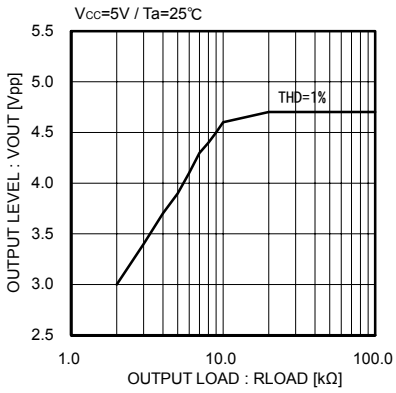


Fig.12 Delay side output load drive characteristic

●**Reference data**

＜BU9262AFS＞

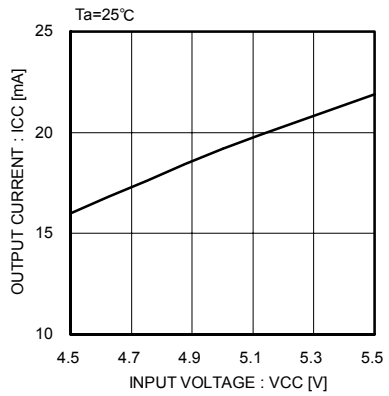


Fig.13 Circuit current

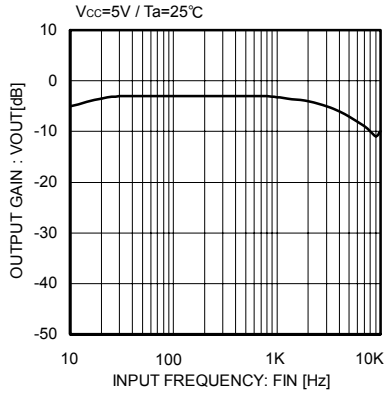


Fig.14 PRE FILTER frequency characteristic

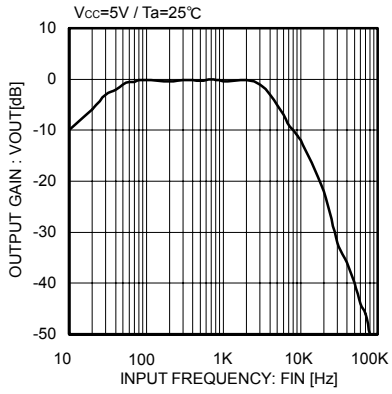


Fig.15 FBVOL frequency characteristic

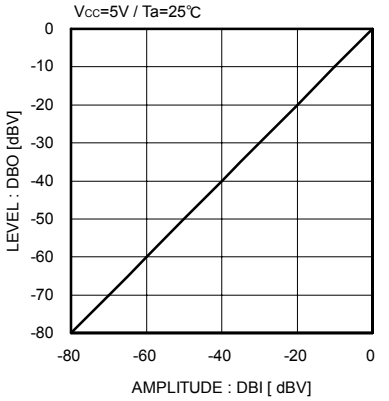


Fig.16 Line amplifier linearity

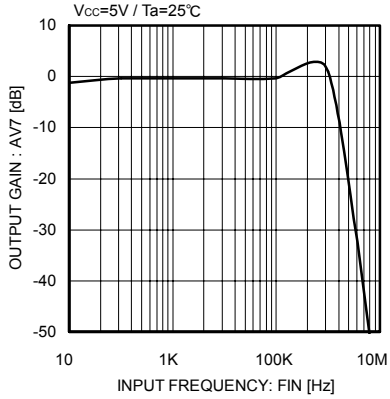


Fig.17 Line amplifier frequency characteristic

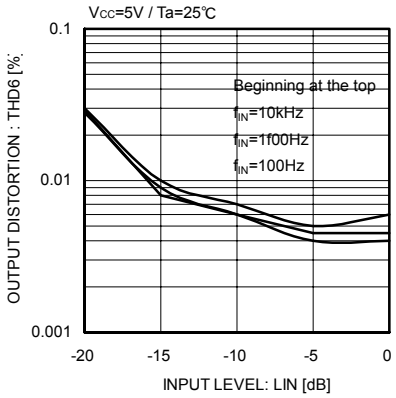


Fig.18 Line amplifier distortion characteristic

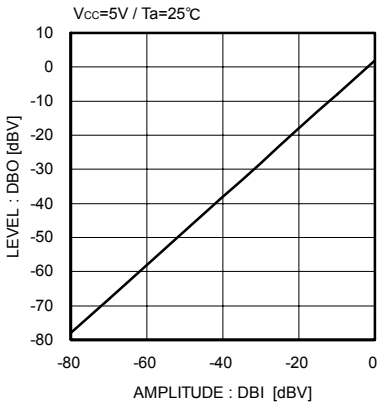


Fig.19 MIX VOL linearity

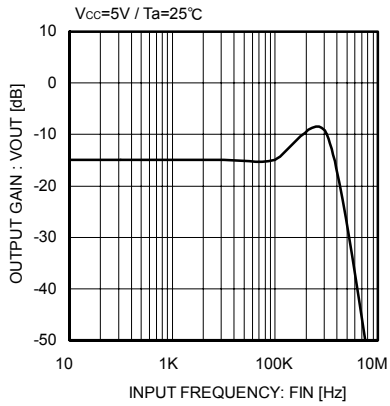


Fig.20 MIX VOL frequency characteristic

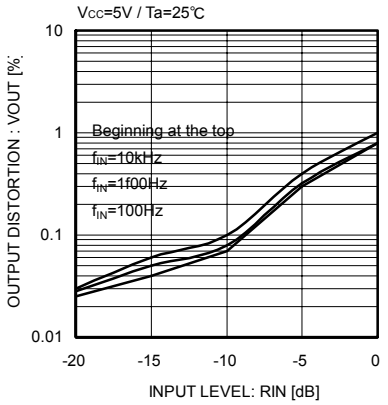


Fig.21 MIX VOL distortion characteristic

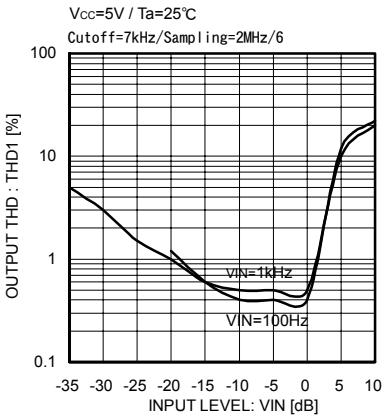


Fig.22 Input level vs distortion ratio characteristic 1

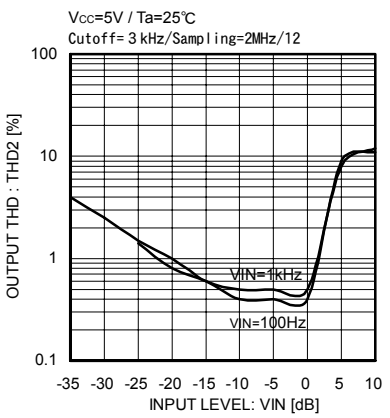


Fig.23 Input level vs distortion ratio characteristic 2

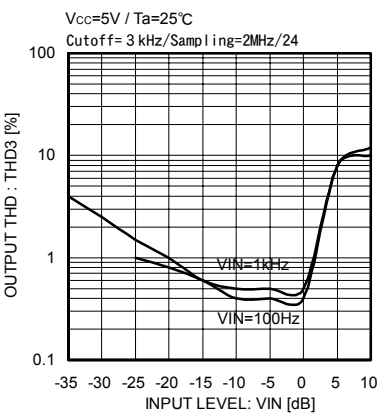


Fig.24 Input level vs distortion ratio characteristic 3

●Pin description, Block diagram, Application circuit

＜BU9253AS/FS＞

・Description of terminal

BU9253AS Pin No.	BU9253FS Pin No.	Symbol	Function
1	1	GND	GND pin
2	2	ECHO VR	Echo level DC control pin
3	–	NC1	Not connected
4	3	BIAS	Analog unit DC bypath pin
5	4	DAINT IN	DA side integrator input pin
6	5	DAINT OUT	DA side integrator output pin
7	6	DALPF IN	DA side LPF input pin
8	7	DALPF OUT	DA side LPF output pin
9	8	MIX OUT	Mixing output of original sound and echo sound
10	9	MIX IN	Original sound input pin of mixing amplifier
11	10	ADLPF IN	AD side LPF input pin
12	11	ADLPF OUT	AD side LPF output pin
13	12	ADINT OUT	AD side integrator output pin
14	13	ADINT IN	AD side integrator input pin
15	14	VCC	VCC pin
16	–	NC2	Not connected
17	15	MUTE	Mute control pin
18	16	CR	Oscillator CR pin

・BU9253AS pin assignment

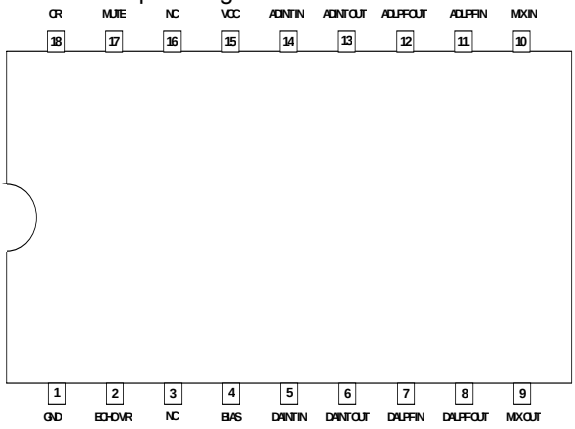


Fig.25 BU9253AS pin assignment

・BU9253FS pin assignment

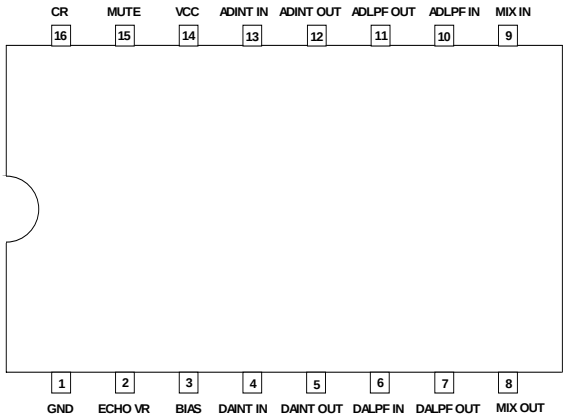


Fig.26 BU9253FS pin assignment

・BU9253AS Block diagram, Application circuit

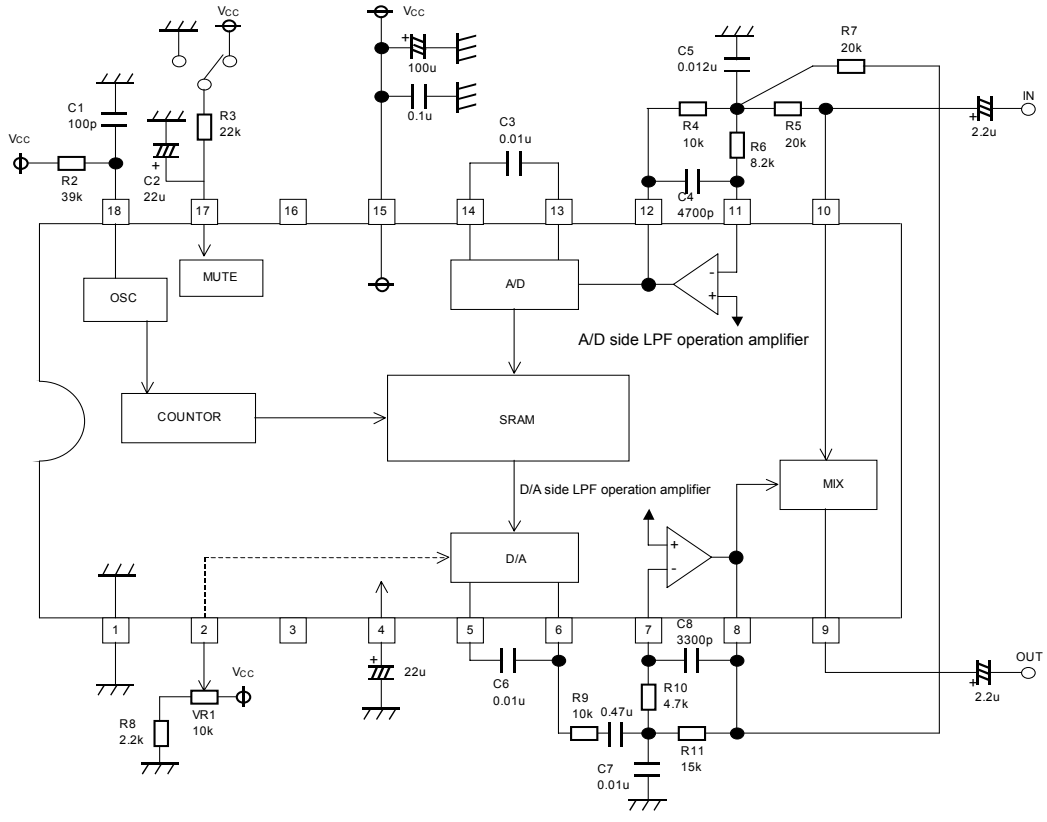


Fig.27 Application circuit

●Pin description, Block diagram, Application circuit

＜BU9262AFS＞

・Description of terminal

No.	Symbol	Function
1	NC	Not connected
2	TESTB	Test negative logic input pin (normally “H” input)
3	SCK	Serial clock input
4	SLT	Serial latch input
5	SI	Serial data input
6	CLKO	Oscillation output pin
7	CLKI	Oscillation input pin
8	NC	Not connected
9	DSOUT	Delay source output
10	TESTOUT	Test output pin (normally “L” output)
11	LPF1I1	LPF capacitor external pin
12	LPF1I2	
13	LPF1O	
14	ADI	ADC capacitor connection pin
15	ADO	
16	GND	GND pin
17	DAI	DAC capacitor connection pin
18	DAO	
19	LPF2I1	LPF capacitor external pin
20	LPF2I2	
21	LPF2O	
22	VOIN	Delay signal / volume input pin
23	DSIG	Delay signal output
24	VREF	Analog reference voltage
25	RCOUT	Rch output
26	LCOUT	Lch output
27	FBOUT	Feedback signal output
28	RCIN	Rch input
29	LCIN	Lch input
30	VCC	Power source pin
31	MICIN	Microphone input (microphone amplifier output connected)
32	MIXIN	Mix signal input

・Block diagram

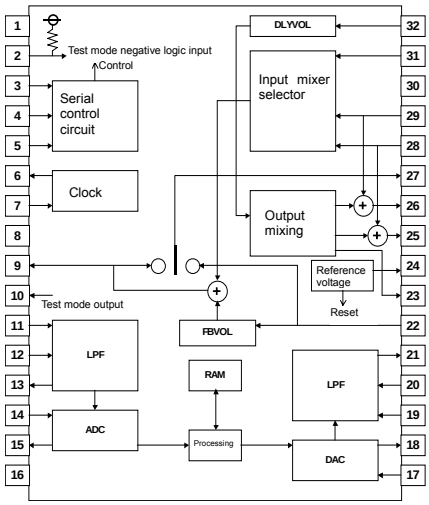


Fig.28 Block diagram

・Pin assignment

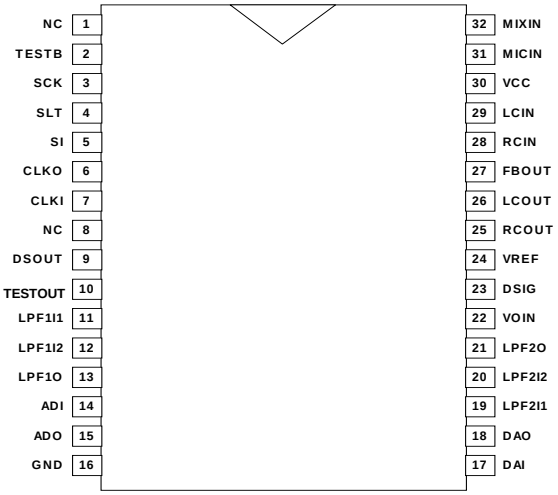


Fig.29 Pin assignment

・Application circuit

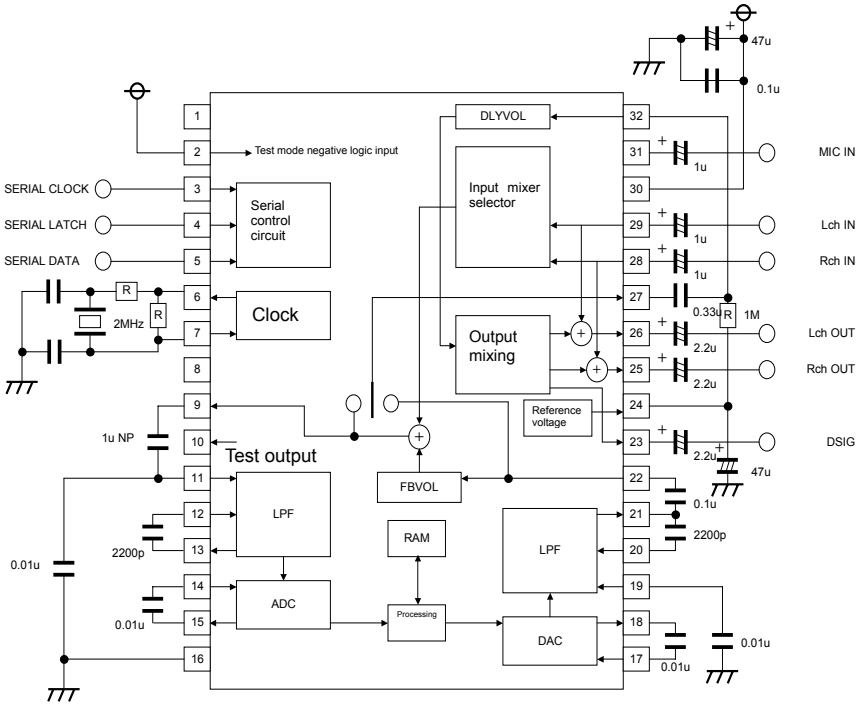


Fig.30 Application circuit

●Description of operations

＜BU9253AS/FS＞

・OSC(Oscillator)

Clock is generated by connecting external RC circuit. Clock is used for the delay counter.

・Mute control circuit (MUTE)

By input voltage of the mute terminal, 3 statuses, that is, mute, mute release (operating), and clock stop & mute can be selected.

・COUNTER

This counter is for generating delay time. It can generate delay time about 131ms at oscillation frequency Fclk = 375kHz.

・SRAM

SRAM with 8Kbit capacity for generating the delay.

・A/D side LPF operation amplifier

LPF can be structured by external RC, and band limit of signal to be input to A/D is available.

・A/D

This digitalizes output signal of AD side LPF, and outputs it to SRAM.

・D/A side LPF operation amplifier

LPF can be structured by external RC, and band limit of signal to be output to D/A is available.

・D/A

This converts delayed audio digital data input from SRAM into analog signal.

・Mixing amplifier (MIX)

This circuit is used for mixing delayed signals and (original sound) signals input from MIX IN.

＜BU9262AFS＞

・Serial control circuit

This serial I/F circuit is for setting each register. It can be controlled by serial 16bit data. It reads in SI at the rise of SCK, and latches data at the rise of SLT.

No.	Mode	Remarks
D0	Delay time	Delay time setting "Refer to the separate table."
D1		
D2		
D3	INPUT select “ISEL”	(D3、D4) = (L、L) : L＋R (L、L) : L－R (L、H) : MIC (H、H) : CLK OFF
D4		
D5	OUTPUT select “OSEL”	(D5、D6) = (L、L) : FWD (L, R in phase) (L、L) : REV (R in opposite phase) (L、H) : MIC MIX (H、H) : NORMAL
D6		
D7	Delay out “DOSW”	H : output ON L : output OFF
D8	Delay volume “DLYVOL”	Delay signal / volume setting "Refer to the separate table."
D9		
D10		
D11	Feedback volume “FBVOL”	Feedback / volume setting "Refer to the separate table."
D12		
D13		
D14	Latch control	(D5, D6) = (L, H) : latch Others are not latch

・Delay time control circuit

This circuit controls delay time. -8 delay time can be selected by register.

D0	D1	D2	Delay time (Sampling frequency)	LPF cutoff frequency
L	L	L	9.2msec (2MHz / 6)	7kHz
H	L	L	15.4msec (2MHz / 6)	
L	H	L	21.1msec (2MHz / 6)	
H	H	L	30.0msec (2MHz / 6)	
L	L	H	48.0msec (2MHz / 6)	
H	L	H	96.0msec (2MHz / 12)	3kHz
L	H	H	144.0msec (2MHz / 18)	
H	H	H	192.0msec (2MHz / 24)	

・Delay signal volume circuit

This is the delay signal volume circuit. 8 volume setting can be selected by register.

D8	D9	D10	DLYVOL
L	L	L	+3dB
H	L	L	0dB
L	H	L	-3dB
H	H	L	-6dB
L	L	H	-9dB
H	L	H	-12dB
L	H	H	-15dB
H	H	H	-∞dB

・Feedback volume circuit

This is the feedback volume circuit. 8 feedback volume setting can be selected by register.

D11	D12	D13	FBVOL
L	L	L	-3dB
H	L	L	-5dB
L	H	L	-7dB
H	H	L	-9dB
L	L	H	-11dB
H	L	H	-13dB
L	H	H	-15dB
H	H	H	-∞dB

・Input mixer・selector circuit

This mixes MIC IN, LCIN, RCIN, VOIN signals, and selects the output path by selector.

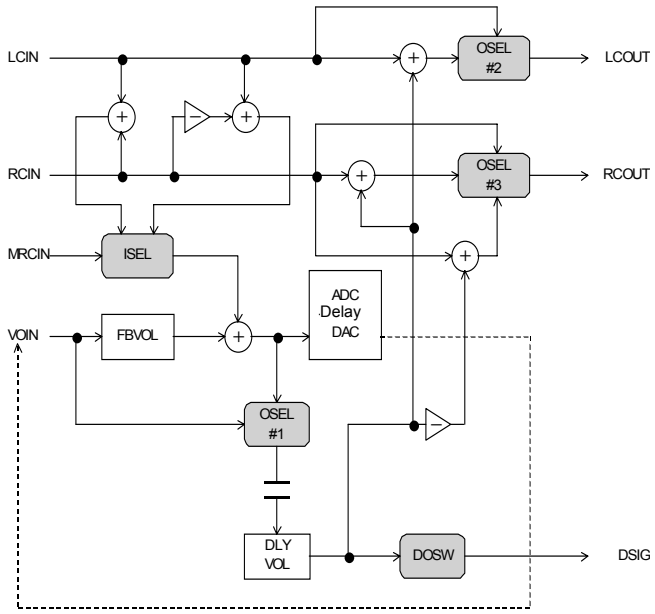


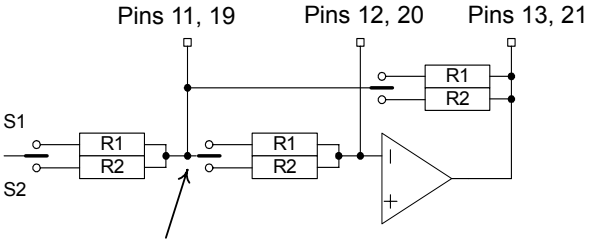
Fig.31 Input mixer selector circuit

・Output/ input LPF circuit

This is the LPF circuit connected to the ADC input unit and the DAC output unit. Delay time setting can be select by internal resistor.

Delay amount	Switch	Resistance value
48.0msec or below	S1	4.8kΩ*
96.0msec or below	S2	11.3kΩ*

*Internal resistance precision is ±30%.



Note: In Pin 11, is an external capacity connection

Fig.32 Input LPF / Output LPF circuit

・Auto mute circuit

Delay output is muted during power on and delay time switching.

●Timing chart

＜BU9262AFS＞

・Serial interface specification

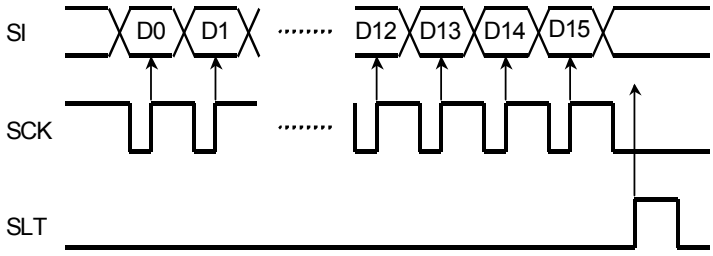


Fig.33 Serial interface specification

・Serial timing

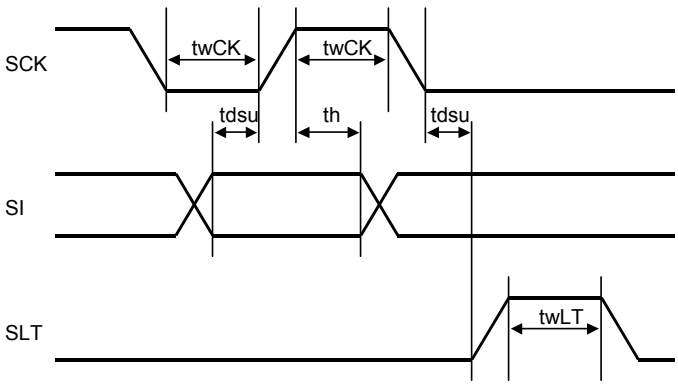


Fig.34 Serial timing

●Description of external components

< BU9253AS/FS > (Refer to Fig. 27.)

・Echo level

Echo signal level is determined by the gains of A/D side operation amplifier and the D/A operation amplifier, since there is no gain in A/D → SRAM → D/A. Path in applied circuit example,

Gain at A/D side : R4 ÷ R5 = 10K ÷ 20K = 0.5

Gain at D/A side : R11 ÷ R9 = 15K ÷ 10K = 1.5

When the original signal is defined as 1, the echo signal level becomes the feedback ratio.

Echo signal feed back ration = 0.5 x 1.5 = 0.75 = 75%

・Echo level setting method

Echo level can be set by adjusting DC voltage by VR1. It does not change in low voltage range, therefore, R8 is added, and it can be adjusted by VR pot.

・Clock frequency and delay time

Clock frequency and delay time are as the following equations.

Sample frequency = clock frequency ÷ 6

Delay time = (1 ÷ sample frequency) x 8192 (SRAM 8192 bits)

As an example, when clock frequency is 375kHz, then sample frequency is 375kHz ÷ 6 = 62.5kHz. Therefore, the delay time is:

Delay time = (1 ÷ 62500) x 8192 = 131ms

Clock frequency is determined by R2, C1 connected to CR terminal (pin 18 in BU9253AS, pin 16 in BU9253FS). When C, R are changed, oscillation frequency changes, but the delay time is kept fixed.

・LPF frequency characteristic

When the band width is set too narrow, echo voice becomes worse, and when band width is set wide, A/D cannot be converted, and S/N becomes worse. Band width of applied circuit example is 2kHz.

・A/D, D/A external capacitors C3, C6

Feedback is set by resistance and capacitor so that output follows even when input signal level and frequency of A/D, D/A change. Variation in the externally attached capacitor can influence the sound quality. A small capacitor can generate noise, while a capacitor that is too large will attenuate. In applied circuit example, 0.01uF is selected to avoid influence upon LPF.

・Mute

Can be controlled by input voltage of MUTE pin. It takes more than one SRAM cycle for switching between mute → mute release (L → M → H). It is necessary for initializing SRAM and insuring stable status before changing operating modes. MIX OUT output is muted, so original sound and echo sound output is stopped.

MUTE pin	Mode
H	Mute release (operating)
M	Mute
L	Clock stop & mute

In the applied circuit example, MUTE is set by R3, C2. In the specifications, voltage range of M is 1.6V ~ 2.8V, therefore, it is necessary to change R3,C2, and set the time of 1.6V ~ 2.8V over 131ms. In consideration of fluctuation, C2 = 22uF, R3 = 22kΩ. When MUTE pin is controlled by the microcontroller, select M range to 1.6V ~ 2.8V and keep M level over 131ms.

・Maximum signal input

When original signal and echo are in phase and mixed, both the signals are added to reach maximum output. In order not to clip this signal, the maximum output at power source voltage of 5V is about 4Vpp. When echo feedback ratio is 0.75, then maximum signal input becomes about 1.0Vpp.

$$\text{Vout MAX} = 1 / (1 - A) \times \text{Vin}$$

$$= 1 / (1 - 0.75) \times \text{Vin} = 4\text{Vpp}$$

$$\therefore \text{Vin} = 1\text{Vpp}$$

・LPF and echo system gain

When the ratio of original signal and echo is changed, R5, R6, R9, R11 are also changed, and the characteristics of LPF change too. Therefore, it is necessary to change all the constants of LPF. In the case, to precisely measure the ratio of original signal and echo, remove R7, input signal around 500Hz without the influence of LPF from MIX IN, and compare it with the output of DALPF OUT.

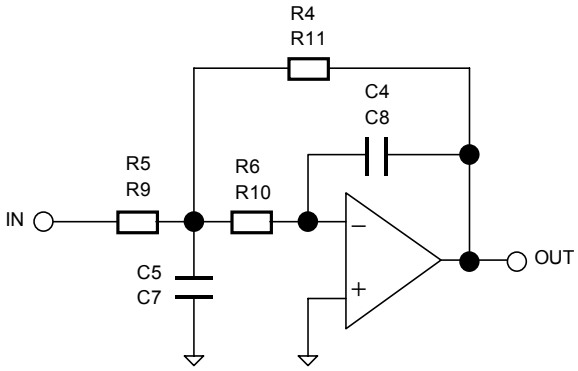


Fig.35 LPF and echo system gain

$$fc = \frac{1}{2\pi\sqrt{C_4 C_5 R_4 R_5}}$$

$$Q = \frac{1}{R_4 R_5 + \frac{R_4 R_5}{R_6}} \sqrt{\frac{C_5 R_4 R_5}{C_4}}$$

Q generally about 0.7

$$A_1 = \frac{R_4}{R_5} \qquad A_2 = \frac{R_{11}}{R_9}$$

Echo signal amplitude ratio

$$= A_1 \times A_2 = \frac{R_4 \times R_{11}}{R_5 \times R_9}$$

・Clock oscillation

As for C,R, tolerance should be below 5%. Note: If measurement is made by attachment a probe oscilloscope it might load the oscillator and reduce the oscillation frequency.

* The set values in this document are for reference only. In the actual set, characteristics may change according to board layout, wiring, types of parts used, and therefore, in actual use, carry out sufficient verification with the actual devices.

●Cautions on Use

1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Operating conditions
Characteristics are guaranteed under the conditions of each specified parameter.

3) Reverse polarity connection of the power supply
Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

4) Power supply line
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks.
Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

5) GND voltage
Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals (except SWOUT) should be lower than the GND potential voltage including an electric transients.

6) Short circuit between terminals and GND or other devices
Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

7) Operation in a strong electromagnetic field
Using the ICs in a strong electromagnetic field can cause operation malfunction.

8) Inspection with set PCB
During testing, turn on or off the power before mounting or dismounting the board from the test Jig.
Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.

9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and breakdown of the input terminal. Therefore, pay thorough attention not to apply a voltage lower than the GND to the input terminals. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply a voltage lower than the power supply voltage to the input terminals, or a voltage within the guaranteed value of electrical characteristics.

10) Ground wiring pattern
The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

11) External capacitor
When using external ceramic capacitors, consider degradation in the nominal capacitance value due to DC bias and changes in the capacitance with temperature.

●**Product designation**

B	U	9	2	5	3	A	S	-	E	2

Part Number
BU9253

Package type
AS: SDIP18
FS: SSOP-A16

Package and forming specifications
E2: Embossed tape and reel

B	U	9	2	6	2	A	F	S	-	E	2

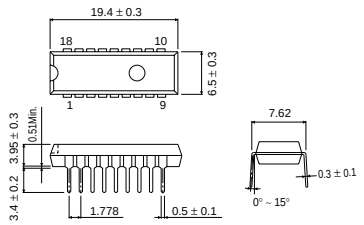
Part Number
BU9262A

Package type
FS: SSOP-A32

Package and forming specifications
E2: Embossed tape and reel

SDIP18

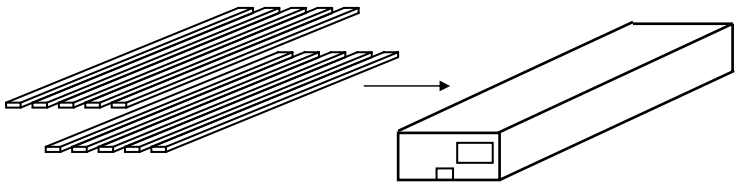
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(Unit:mm)

<Packing information>

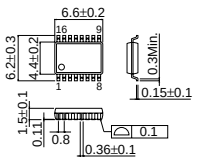
Container	Tube
Quantity	1000pcs
Direction of feed	Direction of products is fixed in a container tube.



※Orders are available in complete units only.

SSOP-A16

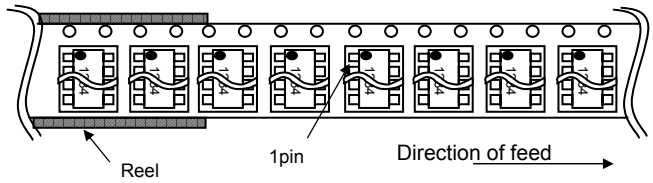
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(Unit:mm)

<Tape and Reel information>

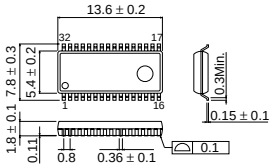
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (Correct direction: 1pin of product should be at the upper left when you hold reel on the left hand, and you pull out the tape on the right hand)



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SSOP-A32

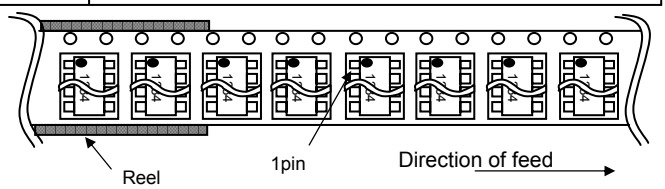
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(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (Correct direction: 1pin of product should be at the upper left when you hold reel on the left hand, and you pull out the tape on the right hand)



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